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SETA Support for the DARPA Microelectronics Technology Insertion Program of the Microelectronics Technology Office

QUARTERLY TECHNICAL REPORT

For the Period
1 August 1992 to 31 October 1992

Sponsored by:
Defense Advanced Research Projects Agency
Microelectronics Technology Office
Microelectronics Technology Insertion Program
ARPA Order No. 8500 Program Code Nos. 2E20 and 2D10
Issued by DARPA/CMO under Contract No. MDA972-92-C-0029

Prepared By:

Daniel H. Butler, Jr.

Approved By:

Robert Swistak

15 February 1992

Booz·Allen & Hamilton Inc.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 February 1993	Quart. Tech. Rep. -1 Aug. 92 - 31 Oct.92

4. TITLE AND SUBTITLE
Quarterly Technical Report No.3 - SETA Support for the DARPA Microelectronics Technology Insertion Program of the Microelectronics Technology Office

5. FUNDING NUMBERS
MDA972-92-C-0029

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER
N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
DARPA/MTO
3701 N. Fairfax Drive
Arlington, VA 22203-1714

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
DISTRIBUTION STATEMENT A: Approved for public release; distribution is unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

Booz-Allen & Hamilton provides DARPA's Microelectronics Technology Office with a broad range of SETA support under contract MDA972-92-C-0029. This report describes activities during the first quarter of this contract. The main programs supported were: the Digital Gallium Arsenide Insertion Program, the Transition of Optical Processors to Systems (TOPS), the Microelectronics Manufacturing Strategy (MMST) Program, the Flexible, Intelligent Microelectronics Manufacturing Program (FIMM),and the Artificial Neural Networks Technology Program (ANNT). In addition, support was begun to a new High Speed Circuit Design Program.

This report is organized by subtask areas in the statement of work, indicating for each subtask the Task Objectives, General Methodology, Technical Results, and Important Findings and Conclusions. The final section of this report presents a summary and conclusions, and the appendices present trip reports, meeting schedules, and some viewgraphs generated during this quarter of the contract.

14. SUBJECT TERMS	15. NUMBER OF PAGES
DARPA, MTO, Transition of Optical Processors to Systems (TOPS), Microelectronics, Artificial Neural Networks, MMST, FINN, ANN, Gallium Arsenide (GaAs)	85
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

Scientific, Engineering, Technical Assistance Support for the Microelectronics Technology Insertion Program of the Microelectronics Technology Office Defense Advanced Research Projects Agency Quarterly Technical Report For the Period 1 August 1992 - 31 October 1992

1. Introduction

Booz·Allen & Hamilton Inc. provides the Microelectronics Technology Office (MTO) of the Defense Advanced Research Projects Agency (DARPA) with a broad range of Scientific, Engineering, and Technical Assistance (SETA) support under contract MDA972-92-C-0029. This report describes activities during the third quarter of the first year of this contract. The main programs supported were the Microelectronics Manufacturing programs, the Transition of Optical Processors to Systems (TOPS) Program, the Digital Gallium Arsenide Insertion Program, and the Artificial Neural Network Technologies (ANNT) Program.

This report is organized by Statement of Work tasks. It describes the Task Objectives, General Methodology, Technical Results, and Important Findings and Conclusions for each subtask, and includes a final section of this report concerning contractual, administrative, and financial considerations.

2. Task 3.1: Engineering and Technical Support Services

This task involved three subtasks:

- Engineering and Technical Integration and Coordination
- Technical Studies and Assessments
- Technical Documentation.

2.1. Subtask 3.1.1: Engineering and Technical Integration and Coordination

Task Objectives. The objective of this subtask is to serve as liaison for various MTO programs, help identify and develop new programmatic opportunities, and explore pathways for technology transfer.

General Methodology. Booz·Allen serves as a primary liaison between MTO, funded contractors, and the technology community at large for the programs supported under this contract. We maintain regular phone contact with contractors; conduct on-site visits to contractor facilities; and participate in

conferences, workshops, and symposia. Booz·Allen monitors contractor activities through informal on-site visits, workshops, and regularly scheduled In-Progress Reviews.

Technical Results, Findings, and Conclusions. During the third quarter of this contractual effort, Mr. Dan Butler, Booz·Allen program manager, and other Booz·Allen employees met with contractors and other parties involved in Microelectronics Manufacturing and Digital Gallium Arsenide (GaAs) efforts to serve as liaison for MTO and monitor progress toward each program's objectives.

Microelectronics Manufacturing activities included the following:

- Mr. Mark Connor attended the Microelectronics Processing '92 Conference in San Jose, California on 21 September 1992 through 25 September 1992. Appendix A contains a trip report from this conference.

- Mr. Graydon Larrabee reviewed the Sandia Contamination Free Manufacturing (CFM) Center.

- Mr. Larrabee made a presentation on Wet & Dry Cleaning to Sandia National Laboratory.

- Mr. Larrabee attended the Sandia CFM - DARPA meeting.

At the microelectronics processing conference, Mark Connor attended the Advanced Techniques for Integrated Circuit Processing II Subconference on behalf of Mr. Zachary Lemnios. Consideration of etching issues, especially magnetically enhanced reactive ion etching (MERIE), dominated nearly half of that subconference. The problem of microtrenching was also discussed and merited further research, in Mr. Connor's opinion. Cost and technology issues related to multi-chip module (MCM) manufacturing were also reviewed.

Graydon Larrabee reviewed the progress at the Contamination Free Manufacturing center at Sandia National Laboratory, and later made a technical presentation at Sandia on silicon-wafer cleaning. He also met with representatives of Sandia, SEMATECH, and DARPA in Washington. Mr. Larrabee concluded that SEMATECH was driving the research center towards short term, incremental and improvement-type projects, a position in his opinion not acceptable to DARPA or to forward looking American microelectronics manufacturers.

Digital Gallium Arsenide activities included the following:

- On 28 August 1992, Mr. Dan Butler visited Lockheed Sanders to review the current status of their digital GaAs Insertion project. Appendix B contains the trip report of this visit.

- Mr. Butler attended the OH-58D Image Processor Program Status Review in St. Louis, Missouri on 7 October 1992. The financial and programmatic status of this insertion effort were reviewed.

- Mr. Kurt Hinds and Mr. Connor attended the 1992 IEEE GaAs IC Symposium at Miami Beach from 4 October to 7 October 1992. Mr. Hinds also attended a short course on Heterojunction Bipolar Transistor Integrated Circuit (HBT-IC) technology and applications during the conference.

In his position as contractor liaison between DARPA and Lockheed Sanders, Mr. Butler attended the Lockheed Sanders Status Review Briefing on the 126B ECM GaAs Upgrade. Problems Lockheed Sanders was having with the first set of TriQuint chips were discussed as well as proposed solutions; it was noted that **problems with additional TriQuint chips could jeopardize the DARPA program**. Appendix B, Attachment 1 contains the TriQuint analysis of chip failure problems; Attachment 2 presents Lockheed Sanders' memo concerning these problems; and, Attachment 3 provides copies of the viewgraphs of Lockheed Sanders' Program Status Review Briefing and System Upgrade.

Likely candidates for upgrades with the improved AN/ALQ-126 were identified. Even if the Airborne Self-Protection Jammer (ASPJ) is successfully completed, the AN/ALQ 126B upgrade need not compete with the ASPJ, since the Navy has declared it does not intend to retrofit ASPJ into the rest of the fleet. Mr. Butler noted that the administrative responsibility within NAVAIR has changed. Oversight for the program now rests with Mr. A. C. McMullin, the deputy director, Program Manager Air-272 (PMA-272), who may be more sympathetic to a flight test than Mr. William Brockner, the Deputy Director, PMA-253.

2.2 Subtask 3.1.2: Technical Studies and Assessments

Task Objectives. The objective of this subtask is to provide technical expertise for translating microelectronics performance benefits into operational benefits. This requires performing systems analyses and providing background information on technical and programmatic aspects of a wide variety of operational and developmental military systems.

General Methodology. Key personnel used a variety of analytical methods to conduct technical studies and assessments. Expertise available within the team of key personnel was supplemented as necessary by corporate resources and special consultants, in order to provide MTO with the most robust analysis available.

Technical Results, Important Findings, and Conclusions. The paragraphs below describe several study activities initiated under this subtask and their associated findings.

Flexible, Intelligent Microelectronics Manufacturing (FIMM). Booz·Allen personnel continued to provide technical support to the efforts of the MTO Director and MMST Program Manager to create a small, flexible, intelligent wafer fabrication (or "fab") facility by the end of the decade. In this quarter, version 1.0 of the computer model of dynamic random access memory chip (DRAM) manufacturing costs was completed. This model was constructed from past data (1970s, 1980s, and early 1990s), as well as current forecasts, to project DRAM manufacturing costs out to 2004. Execution of the model shows capital costs for wafer fabs will escalate to $2.4 billion for the 4 Gigabit DRAM. Similarly, development costs for that technology node rise to $1 billion while manufacturing costs will increase to $1,958 per wafer. This model illustrates the importance of increasing wafer diameter. Moving to 200 millimeters is essential for the 1990s and 300 millimeters for the 2000s. In the model, development costs were amortized over three wafer fabs under the assumption that a company would spread manufacturing to multiple worldwide fabs. Even with the escalating costs shown in the model, however, the DRAM cost per bit continues down the historic learning curve.

Commercial Uses of Artificial Neural Network Technologies (ANNT). At the request of the ANNT Director, Booz·Allen initiated a study to document current commercial uses of artificial neural networks. Booz·Allen prepared a special technical report that is currently under review. It will be delivered to the ANNT Director early in the next quarter.

Look Back at GaAs. The MTO Director requested an overall review of DARPA's Digital GaAs Insertion programs. For the MTO Program Review in October, Booz·Allen assembled a retrospective briefing on the GaAs Insertion program for the MTO Director. This included retrieving historical presentation material from Booz·Allen's files and querying GaAs contractors on their plans for future uses of the technology. The GaAs Program Manager adopted this briefing for his presentation at the final GaAs workshop on 20 November 1992. Appendix 2 contains a copy of this briefing.

Integrated Circuit (IC) Manufacturing Research. In February 1992, Booz·Allen initiated a concerted effort to study IC manufacturing processes and issues to provide the best possible support to members of MTO staff involved in designing a new DARPA program for microelectronics manufacturing. To this end, as described above, Mr. Connor attended that Microelectronics Processing '92 conference. He began a review of the proceedings of the latest Very Large-Scale Integration (VLSI) Multilevel Interconnect Conference (VMIC) conference as well; both tasks were undertaken at the direction of the Microelectronics Manufacturing Science and Technology (MMST) Program Manager.

Booz·Allen believes that MTO would benefit greatly from a state-of-the-art special technical report on IC processing, and recommends that such a task be established with a completion date of July 1993.

2.3 Subtask 3.1.3: Technical Documentation

Task Objectives. The objective of this subtask is to provide writing, editing, production, and technical document coordination.

General Methodology. The level of support required for this subtask varies according to the needs of the MTO Director and the program managers. Due to the rapid turnaround required for most documentation produced under this subtask, Booz·Allen generally schedules all other less urgent tasks around the generation of these documents.

Technical Results, Important Findings, and Conclusions. Technical documentation generated this quarter included the production of view graphs and briefings. In addition, Booz·Allen personnel reviewed articles to be submitted for publication, and the content of a Broad Agency Announcement (BAA) for a new MTO High Speed Circuit Design Program.

Viewgraphs and Briefings. A total of 60 new and revised viewgraphs were produced during the third quarter. Many of these taskings required rapid turnaround and absorbed a significant portion of available resources. A majority of them were required for the MTO Program Review in late October. Booz·Allen delivered thirty bound copies of this review on 19 October 1992.

Booz·Allen also created briefings on the funding history and performance of the Martin Marietta Radio Frequency (RF) Hellfire GaAs Digital Signal Processor (DSP) program and the McDonnell Douglas GaAs Insertion OH-58D Image Processor program. Both these tasks were performed at the direction of the Digital GaAs Insertion Program Manager.

Article Reviews. At the MMST Program Manager's request, Booz·Allen summarized 14 articles that had been submitted to the program manager. Booz·Allen delivered these summaries to the MMST Program Manager, with recommendations concerning which articles merited his further review. Many of these articles were subsequently published in the September-October 1992 issue of the TI Technical Journal.

Editorial Assistance. Booz·Allen proofread a proposed MTO Broad Agency Announcement (BAA) for clarity of substance, as well as for errors of spelling, grammar, and punctuation.

Special Comments, Implications for Further Research. The level of effort required for this subtask had dropped during the last quarter, because most MTO personnel were at the DSRC in La Jolla, California, for most of July. During this quarter, however, demand increased and was particularly intense around the time of the MTO Program Review, when all other tasks were deferred until the briefing was completed. Periods of high demand for these services are expected to continue throughout the period of performance. To ensure rapid turnaround, Booz·Allen will continue the general approach of scheduling all other, non-urgent taskings around those requiring rapid turnarounds.

3. Task 3.2: Management and Administrative Support Services

This task contains five subtasks:

- Program Planning and Control
- Facilities and Logistics Support
- Documentation Management and Control
- Administrative Program Support
- Transition Plan/Scheduling/Phasing

3.1 Subtask 3.2.1: Program Planning and Control

Task Objectives. The objective of this subtask is to provide MTO with planning and control assistance. It includes (1) providing schedule and resource visibility to ensure that contract objectives are being achieved, and (2) tracking performance, schedule, action items, and subcontracted efforts.

General Methodology. Activities in this subtask complement efforts in Subtask 3.1.1 (Engineering and Technical Integration and Coordination) and are carefully coordinated to ensure complete follow-through on action items.

Technical Results, and Important Findings and Conclusions. During the third quarter of this contractual effort, Booz·Allen personnel performed valuable program planning and oversight functions for MTO. Much of this work was done for the FIMM, GaAs Insertion, and TOPS programs, as well as the new High Speed Circuit Design Program.

FIMM Program. As previously noted, Booz·Allen personnel traveled to Albuquerque, New Mexico to review the technical direction of the SEMATECH-funded CFM Research Center. A technical presentation was made at Sandia on "Cleaning of Silicon Wafers" emphasizing the need to work on all-dry cleaning and processing. Meetings were held in Washington and Dallas with Mr. Zachary Lemnios, Mr. Robert Blewer and Mr. Charles Gwyn of Sandia and Mr. Eugene

Feit of SEMATECH to move R&D to leading-edge technologies. Considerable progress was made, and now Sandia has all-dry cleaning ranked as a top priority program. Nevertheless, much more work is required to establish Sandia as a world-class CFM research center.

GaAs Insertion Program. Mr. Butler attended a review at Lockheed Sanders in late August. Results of this trip are discussed under Subtask 3.1.1 and Appendix B. Booz·Allen arranged a classified meeting for 4 November 1992 between the representatives of Lockheed Sanders and the DARPA GaAs Insertion Program Manager, and Booz·Allen continues to monitor developments in the Lockheed Sanders insertion effort.

High Speed Circuit Design Program. Booz·Allen staff assisted the GaAs program manager to begin a new program on high speed circuit design. Support included rendering technical advice, assisting with the preparation of the (BAA), and suggesting potential program names. In addition, Booz·Allen compiled a database of names and addresses of individuals who were to receive copies of the BAA in early November.

TOPS Program. Booz·Allen personnel assembled a schedule of TOPS demonstrations, informal reviews and IPRs to assist the TOPS Program Manager in planning his schedule over the next year. Appendix D contains a copy of this schedule.

3.2 Subtask 3.2.2: Facilities and Logistics Support

Task Objectives. Under this task, Booz·Allen provides the personnel and resources to conduct unclassified and classified technical conferences and workshops. Our support includes planning and organizing these meetings, mailing registration materials and proceedings, and providing conference materials and audio-visual equipment for these conferences.

General Methodology. Booz·Allen participates in various aspects of conference planning, ranging from limited support to total support, as determined by the role of other participants and as directed by MTO staff. Planning activities include identifying, inviting, soliciting, and registering participants; locating and pricing facilities to secure the optimal location through an informal competitive bidding process; arranging logistics such as catering, equipment rental, conference set up; and providing follow-up as necessary (e.g., generating notes and proceedings to document outcomes, thanking participants).

Technical Results, and Important Findings and Conclusions. This quarter, key personnel planned the final GaAs Insertion Workshop scheduled for 20 November 1992, in Reston, Virginia. Invitations were sent out to former

attendees and other interested parties; the agenda was finalized; and all the necessary meeting room, audiovisual, and catering arrangements were made.

In addition, Booz·Allen has begun assisting the TOPS and Photonics Program Manager with an Optics Review to be held from 8 - 12 February, 1993. Booz·Allen solicited bids, and identified the Hilton Hotel at Hilton Head, South Carolina as the proposed site. Work on this task will be conducted under the Optoelectronics contract, but part of the review will be of the TOPS program, which is supported as a part of this contract.

Booz·Allen also assisted Professor David Casasent of Carnegie-Mellon University in arranging an invitation-only session for TOPS contractors at the 1993 SPIE OE/Aerospace Sensing Conference, which will be held in April in Orlando, Florida. On behalf of Professor Casasent, Booz·Allen solicited information from the TOPS contractors who plan to make presentations at the session

3.3 Subtask 3.2.3: Documentation Management and Control

Task Objectives. The objective of this subtask is to coordinate program documentation activities by building and maintaining accurate databases on programmatic information.

General Methodology. Taskings in this area are designed to support program planning efforts covered in Subtasks 3.1.1 and 3.2.1 and provide MTO staff with maximum visibility and flexibility to manage programs.

Technical Results, and Important Findings and Conclusions. This quarter continued to see important progress on the Financial Tracking System, as well as several smaller databases utilized by the Microelectronics Manufacturing program manager in order to coordinate his programs.

Financial Tracking System. The main effort initiated under this subtask is the design and development of the MTO Financial Tracking System, a relational database designed to track funds expended under all MTO contracts. The overall objective of this database is to provide MTO staff with better oversight on the expenditure of funds so that MTO resources can be more efficiently budgeted, committed, and obligated. The database will also enable MTO staff to identify potential problems or funding shortfalls before crises develop. It will also register the receipt of contract deliverables and track the financial information included in such reports. When deliverables are late or financial data are either missing or incomplete, a letter report will be generated and sent to the delinquent contractor, following approval by the responsible MTO program manager.

During the third quarter, data collected through the Contractor Funding Status Questionnaire was compared to data already collected and a program was written to merge this new information into the Financial Tracking System. This information makes the database much more robust. Dr. Andrew Yang's contracts have been added into the system and reports on the status of his contracts are regularly delivered to him and the COTR. Much of Dr. Barbara Yoon's contract information has been entered into the system as well, and Booz·Allen staff will be meeting with Dr. Yoon's SETA contractor in order to procure the data from their Contractor Funding Status Questionnaires.

Other Document Management Taskings. Other documentation management and control taskings include continued, biweekly updating of a point-of-contact database using FileMaker Pro software for the GaAs and manufacturing programs; transferring a part of that database to the GaAs Program Manager's portable Wizard organizer; and organizing the hard copy GaAs and manufacturing program files. Finally, as previously noticed, Booz·Allen compiled a database of individuals who were to receive a copy of the BAA 93-03 announcement for the GaAs program manager.

3.4 Subtask 3.2.4: Administrative Program Support

Task Objectives. The objective of this subtask is to provide administrative program support for the MTO Director, Deputy Director, and staff.

General Methodology. Many individual taskings in a broad range of areas were accomplished under this subtask.

Technical Results, and Important Findings and Conclusions. Administrative taskings performed during this reporting period included mailing copies of MMST wafer displays to Air Force MMST personnel; arranging for, delivering, and hanging a display of the Martin Marietta GaAs On-Board Processor at DARPA; preparing a mailing list for announcements on a new High Speed Circuit Design Program (see 3.2.1); and obtaining various documents and information related to dual-use technologies and the defense and civilian portions of the federal budget.

3.5 Subtask 3.2.5: Transition Plan/Scheduling/Phasing

Task Objectives. The objective of this subtask is to provide a detailed Transition Plan outlining the strategy and methodology for transitioning the program support services performed under this contract to a follow-on contractor.

General Methodology, Technical Results, Important Findings and Conclusions. The general methodology used to accomplish all taskings was designed to ensure complete documentation of activities and development of stand-alone, easily transferable deliverables (e.g., databases, special technical reports, etc.). The objective in doing this is threefold: it provides MTO with complete records and thereby enhances the ability of MTO staff to manage programs effectively; it causes the development of products and services that can be completely transferred to MTO staff for direct use; and it ensures that transitioning to a follow-on effort will be smooth and efficient.

4. Conclusions

This section summarizes the results of the last quarter of effort under this contract, notes any special problems, and makes recommendations for future work.

4.1 Special Comments

Booz·Allen supplied a high level of support during the third quarter of the first year of the MTO SETA contract. No technical problems were encountered in these support efforts, nor was any significant hardware developed or purchased.

This quarter continued to see significant contributions by Mr. Graydon Larrabee, special consultant to Booz·Allen. He responded to special taskings from the MTO Director related to the FIMM program and reviewed the progress of related work by SEMATECH and Sandia National Laboratory. He also completed the first version of a computer program modeling DRAM manufacturing costs.

Technical problems were noted in two programs being monitored as part of this contract. First, the poor performance of the first batch of TriQuint chips for DARPA's AN/ALQ-126B Upgrade GaAs Insertion Program has the potential to jeopardize the program. Secondly, Graydon Larrabee noted that SEMATECH's preference for short term goals for the Sandia CFM is in opposition to DARPA's desires. As a result, Mr. Larrabee anticipates his role in providing future direction for the Sandia CFM program will be minimal.

4.2 Implications for Further Research and Support

The computer model of DRAM manufacturing costs will be updated and extended to cover logic devices. Mr. Larrabee will travel to Asia to examine

fabrication facilities in Asian countries from 2 November to 16 November 1992. He will also attend the SEMATECH CFM Focus Technical Advisory Board (FTAB) meeting on behalf of the Microelectronics Manufacturing program manager.

Booz·Allen personnel will attend the Government Microcircuit Applications Conference (GOMAC '92) and will produce presentation materials for the FIMM Program Manager for that conference as well. The final Digital GaAs Insertion Workshop will be held at Reston, Virginia, on 20 November 1992, and Booz·Allen will provide a broad level of support, including registering attendees, overseeing room set-up and catering, and preparing and mailing out proceedings. Booz·Allen will continue to monitor the remaining digital GaAs Insertion projects at KOR Electronics, McDonnell Douglas, and Lockheed Sanders. Support will continue to be rendered to the TOPS program as required. This may include attending several reviews and/or demonstrations, as well as facilitating the involvement of TOPS contractors in the Optics Review scheduled for February.

Administratively, the BAA on the High Speed Circuit Design Program will be distributed to a mailing list of 150 names. A database will be established for compiling the evaluators' comments for each preproposal. Similar work will be done for the HBT program manager's new BAA as well. The Financial Tracking System will be extended to cover Dr. Yoon's contracts, and eventually expand to cover the contracts of other program managers at MTO.

As noted previously (in Subtask 3.1.2), Booz·Allen believes that MTO would benefit from a Special Technical Report on the current state-of-the-art in IC processing. It recommends that such a task be established, to be completed in the third quarter of 1993.

APPENDIX A
TRIP REPORT
SAN JOSE, CALIFORNIA
21-25 SEPTEMBER 1992

Trip Report

MICROELECTRONIC PROCESSING 92

San Jose, California

September 21-25, 1992

Mark P. Connor attended the convention at the request of Mr. Zachary Lemnios, DARPA-MTO. The convention consisted of numerous conferences, several short courses, and a technical exhibition. Of these Mr. Connor attended the following:

- Advanced Techniques for Integrated Circuit Processing II Conference,
- Rapid Thermal and Laser Processing Conference, and
- the Technical Exhibition.

The Advanced Techniques for Integrated Circuit Processing II Conference lasted three days and covered the following topics:

- polysilicon dry etching,
- plasma processing of materials,
- plasma process modeling,
- high density plasma sources,
- integrated sensors and control strategies,
- multichamber processing and cluster systems, and
- compound semiconductor device processing.

Several highlights of this conference are presented below. Etching issues, especially with magnetically enhanced reactive ion etching (MERIE), dominated nearly half of the conference. Of the many issues discussed, the increasing problem of microtrenching warranted additional papers. See figure 1 for an actual example of microtrenching.

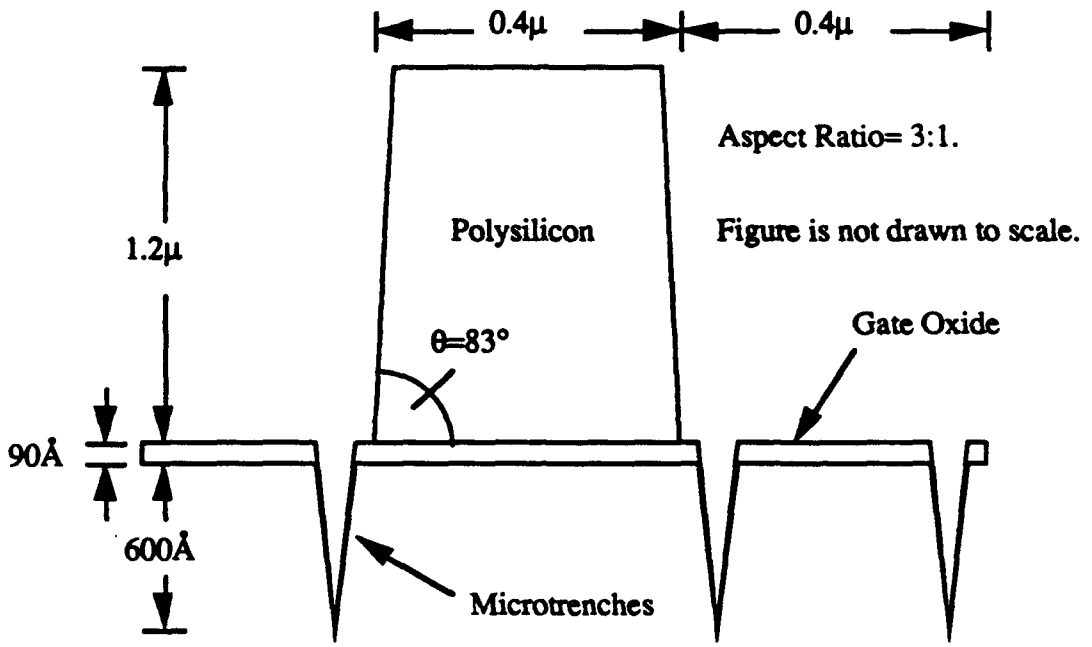

Figure 1. Microtrenching Example.

Microtrenching degrades electrical performance and exacerbates reliability problems. Characteristically, it only is seen between dense or adjacent isolated lines. Moreover, it follows the grain structure of the polysilicon.

Stanford has been investigating the formation of microtrenching, and has established a multiphase, plasma etch model, where understanding intrastructure transport phenomenon, i.e. between lines, is critical. In general, microtrenching is formed by ion reflection from sidewalls, and, to some degree, surface charges. The proposed solutions to the problem include:

(1) reduce the aspect ratio from 3:1 through the use of thin resists on the order of 0.55 μm;

(2) reduce the etch rate of the gate dielectric, possibly using bromine instead of chlorine; and,

(3) collimate the impinging ions with tighter tolerances.

A general consensus throughout the conference was the trend towards the use of the DESIRE process for dry etching. The use of O_2 plasma to remove the photoresist is desired, even though it leaves a sidewall residue. Nevertheless, SiO_3/O_2 plasmas have been demonstrated to perfectly transfer a pattern at 0.275 μm with no dimensional loss. Moreover, such plasmas do not need sidewall passivation.

Some discussion involved multi-chip modules (MCMs). Specifically, the cost drivers in order of priority were identified:

1. quality of ICs -- cost driver for MCMs;
2. IC testing and burn-in, and limited IC testing standards for MCMs;
3. ceramic MCM package -- 99% are made in Japan which takes ~12 weeks to receive;
4. substrate; and,
5. assembly techniques, e.g. flip chip.

The market for MCMs appears to be developing as

- workstations,
- laptop PCs,
- high performance PCs,
- portable telecommunications,
- machines incorporating an asynchronous data and voice transmission mode with high bit rate,
- cross point switches (100Mbit/s - 2.4 Gbit/s),
- DSP applications.

To make MCMs more cost competitive with continually evolving IC technology, one must identify high priority applications (subsystems) for which ICs could not reach the same specifications in a reasonable time frame.

Now, consider the following figure:

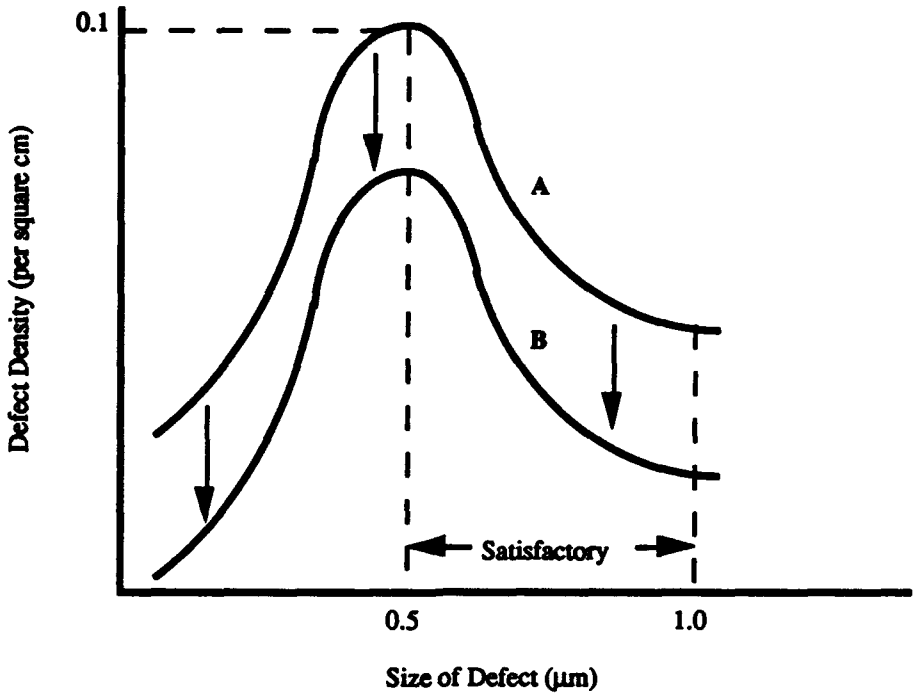

Figure 2. Defect Density vs. Defect Size.

Curve A in Figure 2 is the current situation in MCM manufacturing. Curve B is the desired situation which would eventually eliminate all 1.0 μm defects. This transformation's criticality increases with increasing substrate area. Similar curves and transformations exist for IC manufacturing, but with different scales. The way to achieve this transformation cost effectively in either manufacturing environment is through the use of microenvironments. This is most facilitated with multichamber processing and cluster systems.

Another interesting highlight was the discussion about laser cutting and writing for MCM customization. Such a process allows all but the two interconnect layers to be fully customized and tested from a semi-customized interconnect structure. The x-y signal layers consist of parallel 2 mm line segments which open up to the surface through a via. Thus, a bridge can be made; or, if a bridge exists, an open can be formed. With laser writing or cutting these via jumps, fully customized interconnect structures can be made, as well as low cost repair. Since cutting is quicker than writing, one approach to speed throughput of such MCMs in a high volume manufacturing environment, would be to supply the semi-custom interconnect structure with all the via jumps bridged. Thus, customization results only from laser cutting.

Yields from this approach of 99.9% have been shown with IC compatibility. In fact, a demonstration model involved the Motorola 88100 and two 88200s (f=20 MHz). This 1" x 2" Cu-polysilicon substrate contained three layers with 216 signal interconnect nets. 4000 links were made measuring 20 m$\Omega \pm 7$ mΩ; and, 1600 cuts were made measuring ~ 10^{10} Ω. This MCM safely operated up to 100 MHz, based on wavefront dispersion. Moreover, following the initial writing and cutting, no further rework was required.

The actual Proceedings of this conference are forthcoming. March 1993 is the expected month of publication.

APPENDIX B,
ATTACHMENT 1
TRIQUINT ANALYSIS
NASHUA MEETING
28 AUGUST 1992

An Analysis of failures in the S0972A - DIFM1 Aperture Buffer

by
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for
Ed Wassung
Lockheed - Sanders

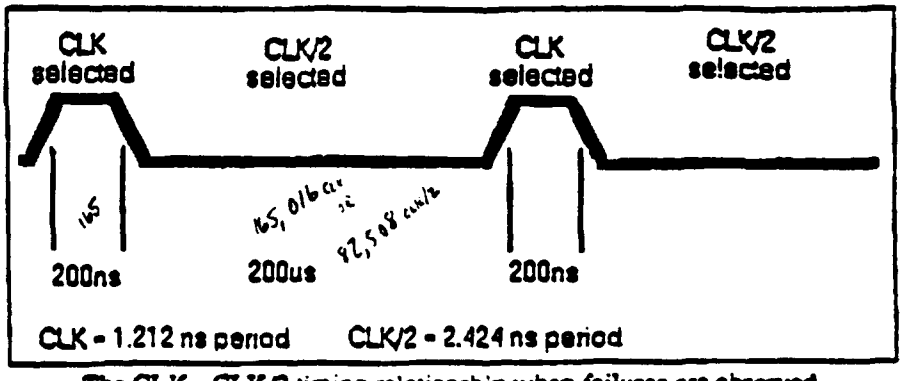
FAX # 603 885 6062

Circuit Description.

The DIFM1 - S0972A Aperture Buffer circuit consists of six 24 stage shift registers accepting data from an on-chip six bit read only memory(ROM). The shift registers are clocked by a clock source consisting of a MUX which selects one of two clock signals, CLK and CLK/2. The CLK signal is selected when the select line is forced HIGH by the negative transition of the CLK signal. Two CLK cycles later the select line HIGH reaches the reset pin of the CLK/2 flip-flop forcing the CLK/2 output LOW. When CLK/2 is selected, the select line is forced LOW by the negative transition of the CLK signal. Two CLK cycles later the select line LOW reaches the reset pin of the CLK/2 flip-flop releasing the CLK/2 output to toggle. Control is given back to the CLK signal immediately after the selection signal is forced HIGH by a negative going CLK edge. Two CLK cycles later the CLK/2 signal is forced LOW by a HIGH to the reset pin of the CLK/2 flip-flop. The MUX drives two clock buffers which in turn drive six more clock buffers. Each clock buffer at the end of this clock tree drives twelve flip-flop stages in one of the six shift registers. For each register the clock driver order is as follows:
buff_1 drives 1,4,5,8,9,12,13,16,17,20,21 and 24 for a total of twelve;
buff_2 drives 2,3,6,7,10,11,14,15,18,19,22 and 23 for a total of twelve.

Operating conditions.

CLK is 825 MHz (a 1.212ns period). CLK/2 is 412.5 MHz (a 2.424ns period).The circuit has been set up such that CLK/2 is always feeding the aperture buffer. At a rate greater than 300KHz, CLK is selected for 200ns and data from the ROM is addressed to provide shift register loading of alternating ones and zeros. After 200ns CLK/2 is again selected and the data is shifted out of the registers, i.e. the signal CLK/2 is selected for 200us. The signal CLK is then selected for 200ns and data is loaded from the ROM into the shift registers. (During the 200ns CLK window CLK/2 is held LOW by the selection signal.) The signal CLK/2 is then reselected and data is shifted out of the registers.



The CLK - CLK/2 timing relationship when failures are observed.

Behavior observed.

When the shift-in shift-out rate is maintained at greater than 300KHz, the circuit behaves correctly, i.e. a pattern of alternating ones and zeros is seen at the output of the shift registers (see attached plot-1 - jul 24 92 - 12:25:49 - rate is 500KHz). As the shift-in shift-out rate decreases, errors begin to show up in the shift register outputs (see attached plot-2 - jul 24 92 - 12:30:51 and plot-3 - jul 24 92 - 12:43:45). The number of shift register stages in error is less when the last sampled bit is a one (plot-3) and greater when the last sampled bit is a zero (plot-2). Except in those cases where errors occur in the first or last shift register stage, good data is present in stages both before and after the stage in error.

From plot-2, trace(tr) 1, errors are in stages 5,13,17 and 21. From tr2, errors are in stages 1,9,13,17 and 21. From tr3, errors are in stages 9, 13, 15,17 and 23. From tr4, errors are in stages 1 and 13. From tr5, errors are in stages 5,13 and 21.

From plot-3, tr1, errors are in stages 5 and 13. From tr2, errors are in stages 9 and 13. From tr3, errors are in stage 1 only. From tr4, errors are in stages 9 and 13. Trace 5 is functional.

Other data from aug 3 92 shows error patterns as follows:

from plot-1 - tr1 shows stages 5,13,17,19,21 in error; tr2 shows stages 1,9,13,17,21 in error; tr3 shows stages 9,13,15,17,21,23 in error; tr4 shows stages 1,13,17,21 in error; tr5 shows stages 5,13,21 in error; from plot-2 - tr1 shows stages 5,13 in error; tr2 shows stages 9,13 in error; tr3 shows stage 1 in error; tr4 shows stages 9,13, in error; tr5 is functional.

Data taken of the shift registers, prior to the CLK/2 signal selection, shows that all data is valid as it progresses under the control of the CLK signal (plot-4). It is only after the CLK/2 signal selection takes place that erroneous data is observed. Errors are occurring in shift register stages that are driven by independant buffers in the clock tree. Errors are occurring in shift register groups 1-3 and 4-6 which are driven by independant buffers in the clock tree. Erroneous shift register output appears to be related to:

1 - the rate at which data is shifted in and out of the registers;

2 - temperature, i.e. when the part is cooled, fewer errors are observed;

3 - (to some extent) the value of the data in the register stage at the time data loss occurred (although errors have been observed when data values were either one or zero); and

4 - frequency, i.e. at f_{CLK} = 800 MHz and selection rate < 300 KHz or at f_{CLK} = 10 MHz and selection rate < 3.7 KHz.

The clock circuitry (as observable from the SDLSYNC output, plot-5) seems to be functioning as expected (it must be understood that there is substantial filtering of the clock signal at this output because of the number of cells in the chain and the bandwidth of the output cell which swamp out

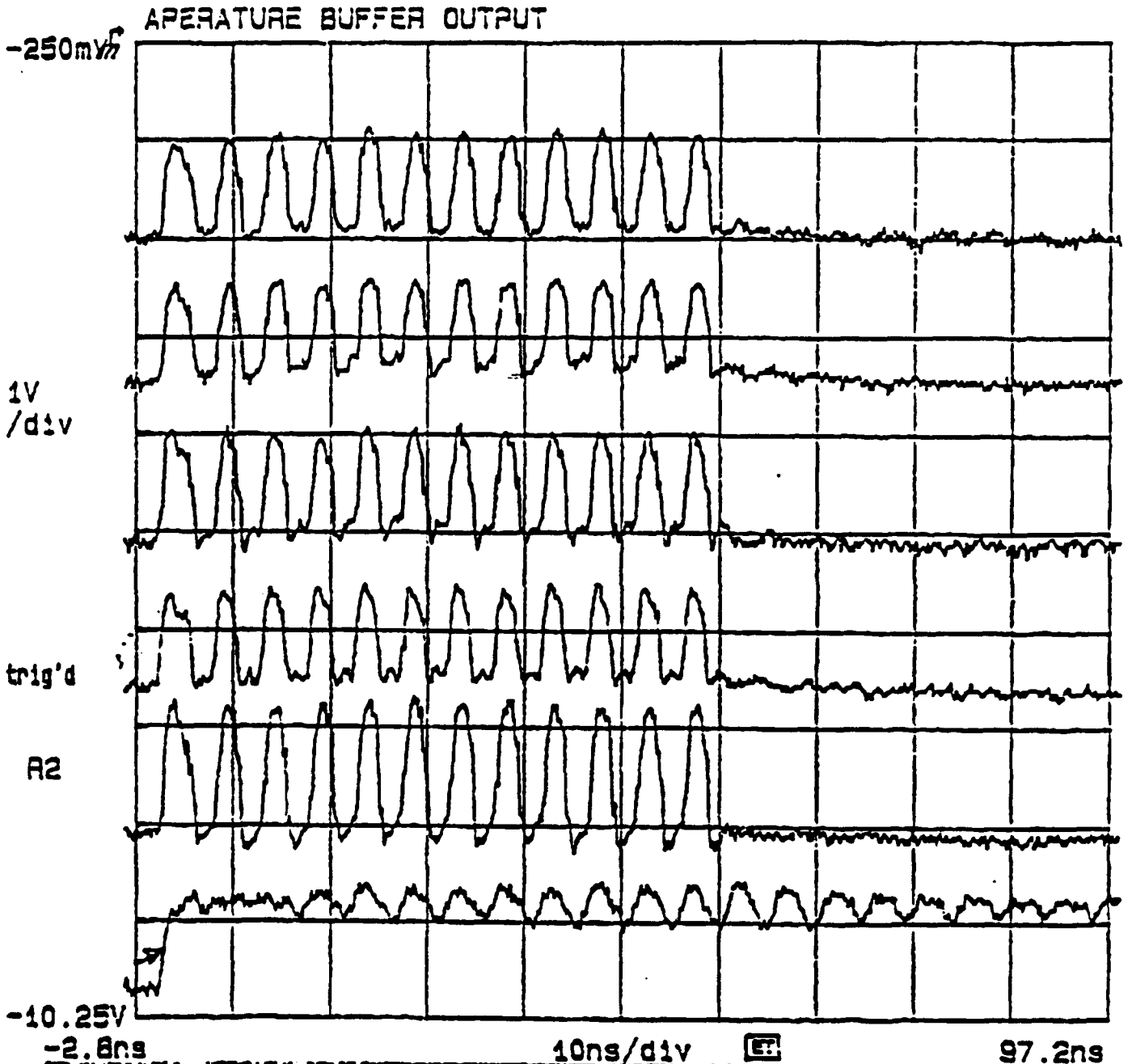
the observability of possible glitch effects).

Analysis.

Since good data is being shifted out (except in the cases where data is lost in the first or last stages) before and after erroneous data, the stage which lost its data must have been functioning correctly both before and after the initial data loss in order for prior and subsequent data to exit the shift register correctly. The data loss must therefore have had to occur at one and only one point in time, after which functionality was restored, in order for prior and subsequent data to be valid. Since data loss is happening to more than one stage in more than one shift register path, the cause must be related to an event which is common to all shift register stages in all shift register paths. Given that all stages are functional during some portion of the shift-in shift-out process, and given that the ciruit function is normal above a certain shift-in shift-out rate, we may conclude that the most likely explanation for data loss in individual stages is that some kind of clock event occurred to cause the data at the input to the stage to pass prematurely to the output of the stage. This event must have happened in a clock path which is common to all shift register stages since data loss is observed in all shift register paths. The only device common to all shift register stage clock inputs is the SF2MUX cell which provides for the selection of the CLK and CLK/2 signals. Also, since data under the control of the CLK signal is always good prior to the CLK/2 selection we can say with certainty that the clock event causing the data loss is the result of either the CLK-to-CLK/2 selection or some fundamental problem with the CLK/2 signal itself. Now, while the CLK/2 signal is selected, no current is flowing through the source coupled FET pair on the CLK side of the SF2MUX, even though the CLK signal is present at the gates of those devices. During the 200ns CLK selection period, alternating one and zero data is shifted into the registers and appears at the output of those registers without error. During this time the CLK/2 signal is forced to a LOW state and no current is flowing through the source coupled FET pair on the CLK/2 side of the SF2MUX.

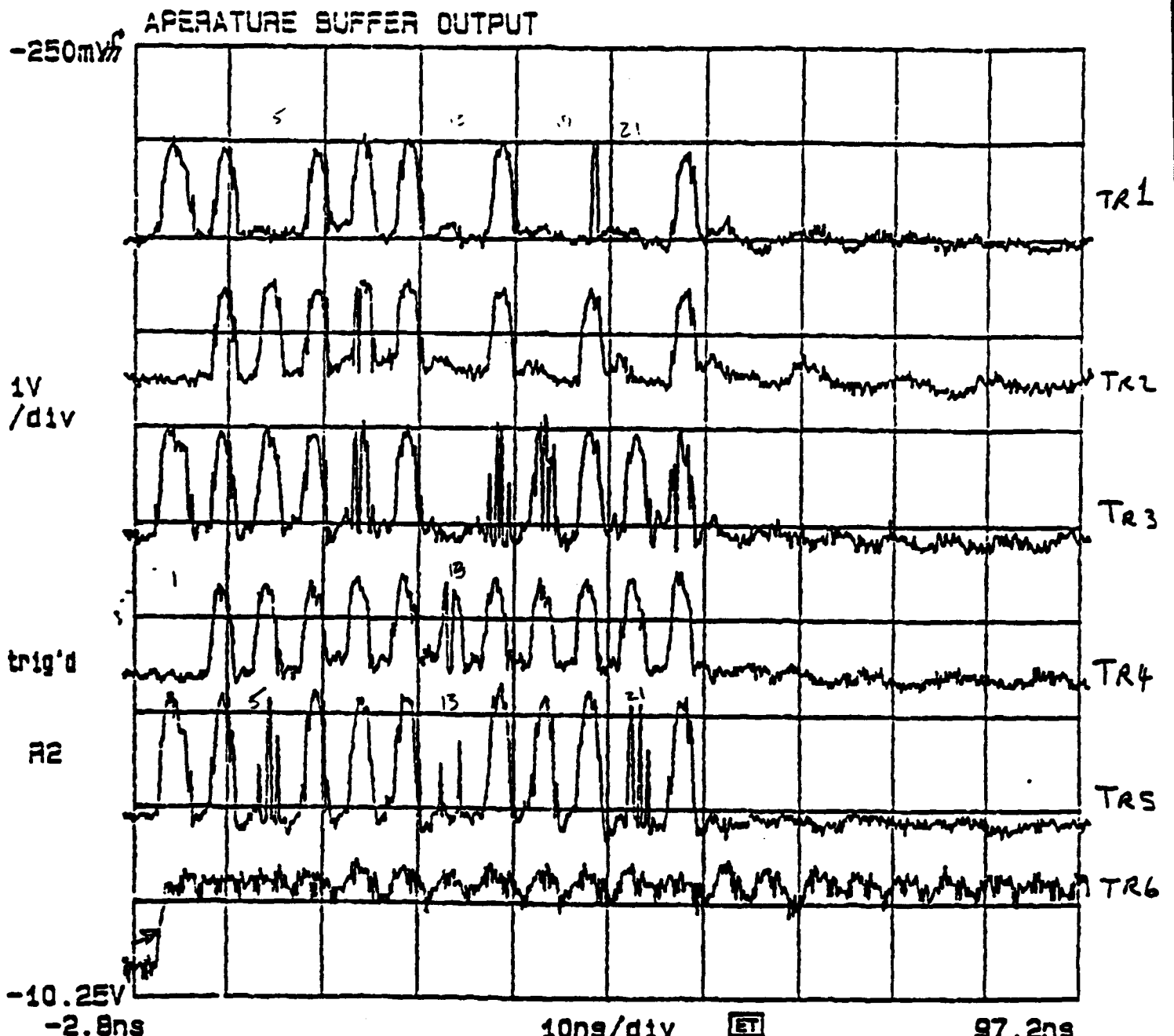
Some questions that immediately surface are:
1 - what is happening in the SF2MUX that could allow for a clock disturbance such that data in the shift registers is affected?; and
2 - what influence does the MUX selection signal have on the output of the MUX, such that a clock disturbance could be possible?

A 602 DIGITIZING SIGNAL ANALYZER
Date: 24-JUL-92 time: 12:25:49



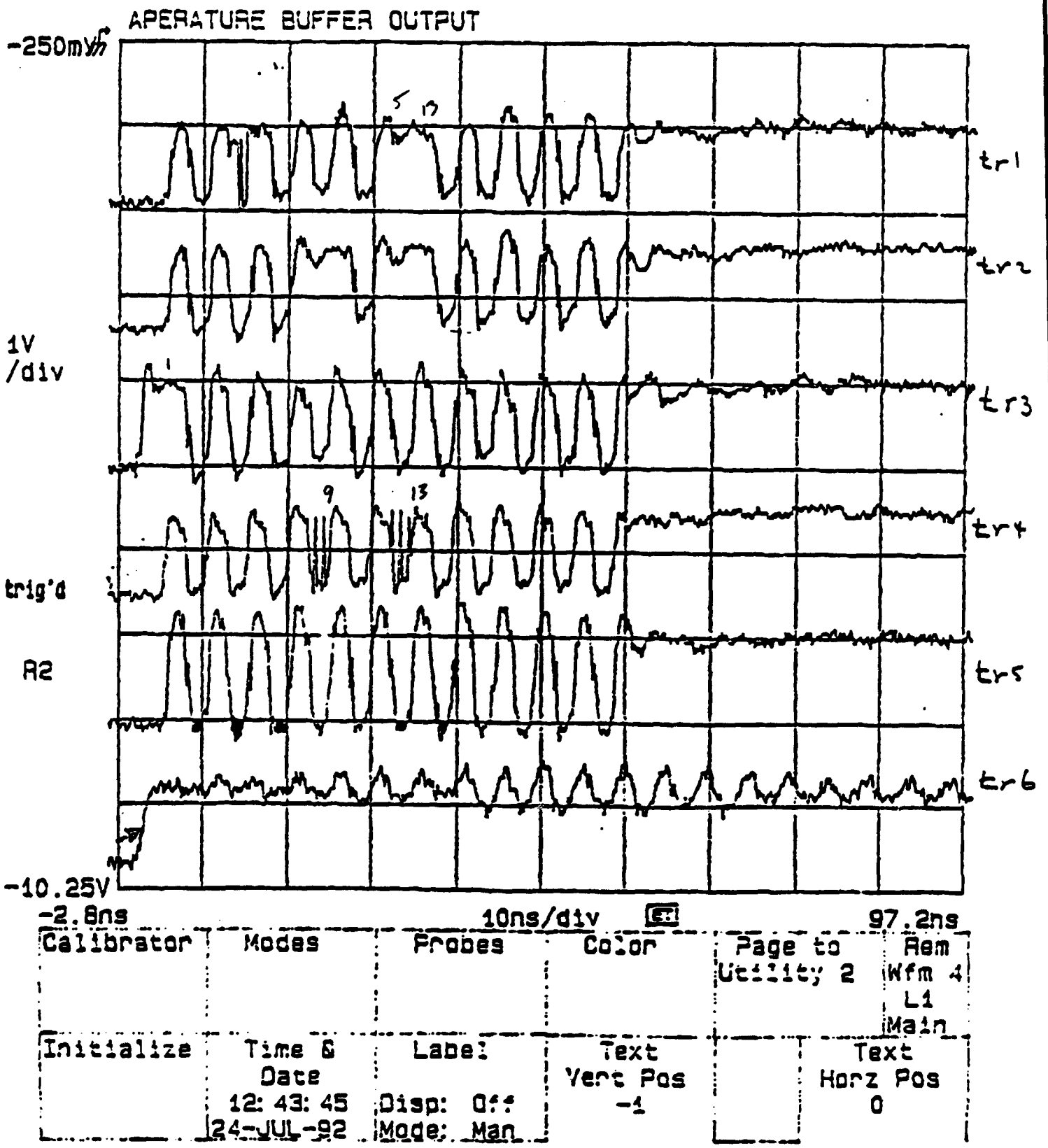
PLOT 1

DSA 602 DIGITIZING SIGNAL ANALYZER
date: 24-JUL-92 time: 12:30:51



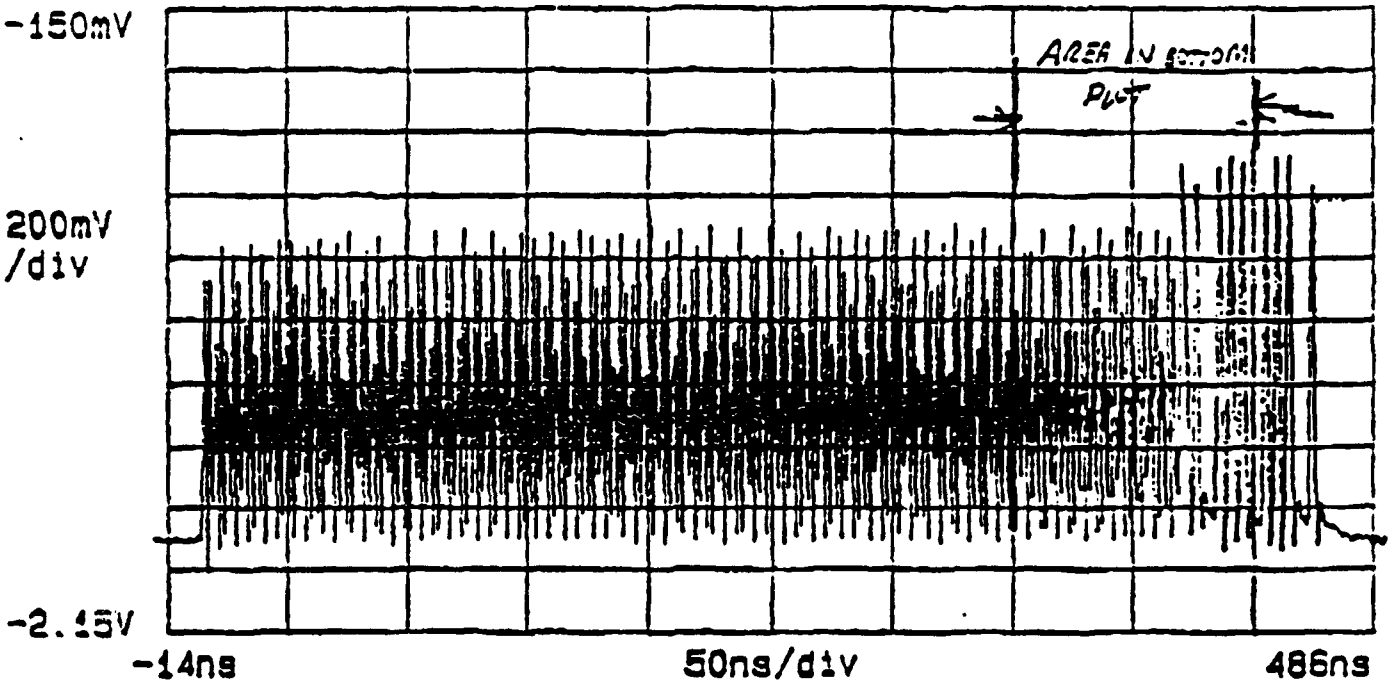
Plot

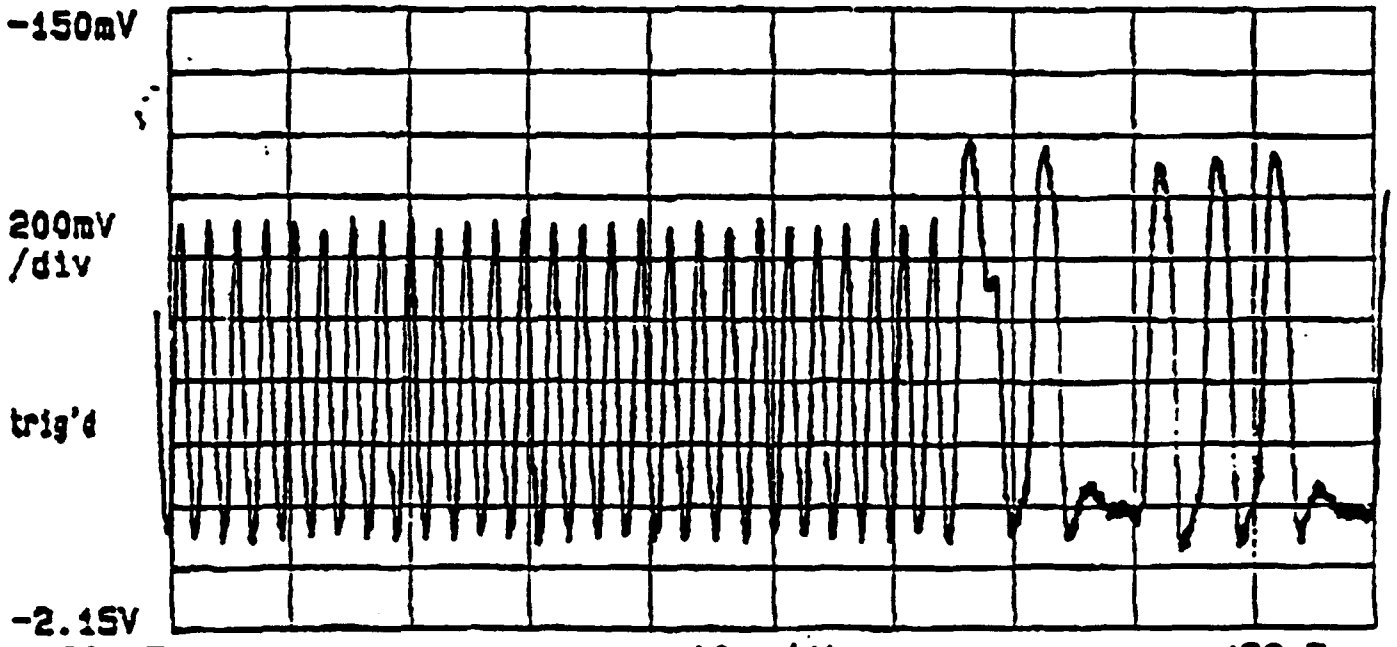
,SA 602 DIGITIZING SIGNAL ANALYZER
date: 24-JUL-92 time: 12: 43: 45



PLOT 3

DSA 602 DIGITIZING SIGNAL ANALYZER
date: 21-JUL-92 time: 14:40:03



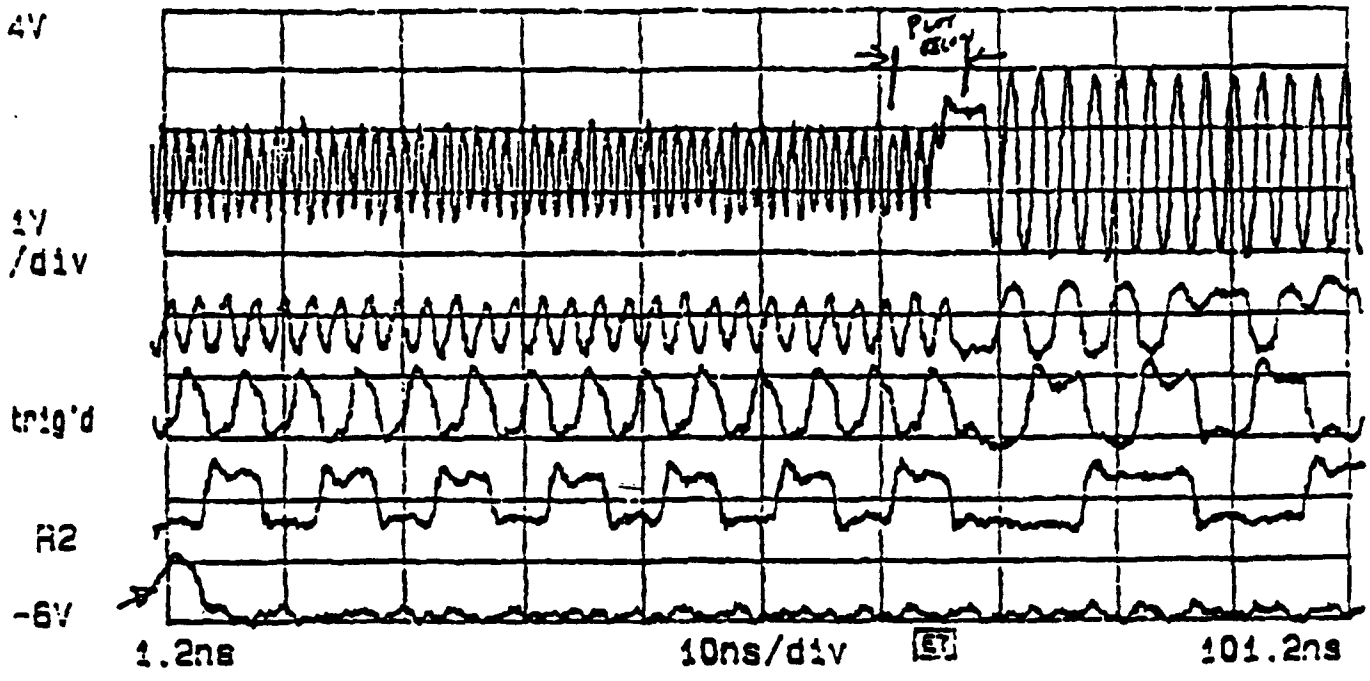


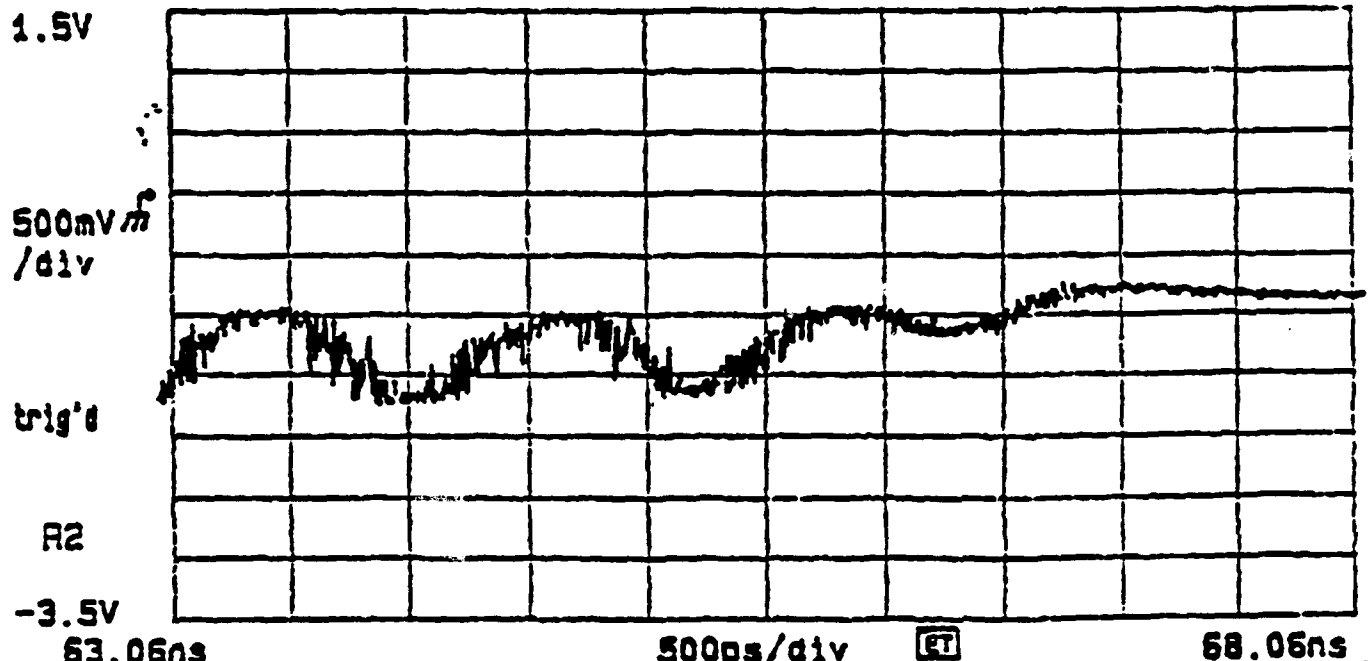
Trigger	Source	Level	Time	Mode	Rem
Select Main	Desc L1	-1.3V	Holdoff 7us	Auto	Wfm 2 L1 Wind

Coupling	Slope	Timer t1 Timer t2
DC	+	6ns 32ns

Plot 4

DSA 602 DIGITIZING SIGNAL ANALYZER
date: 10-AUG-92 time: 16:49:32





GPIB Talk Only 5	RS-232-C 9600 baud	Hardcopy HPGL Screen	Ident	Page to Utility 1	Rem Wfm 7 L1 Wind
Extended Diagnostic	Self Test	Teksecure Erase Mem	Main Trig Level -900mV	Main Trig	Main Time Holdoff 2us

APPENDIX B,
ATTACHMENT 2
LOCKHEED SANDERS ANALYSIS
NASHUA MEETING
28 AUGUST 1992

John M. Lybrain 08/26/92

Lockheed Sanders, Inc Memorandum

To:	Distribution	**File Reference:**	
From:	E. Hollis	EH/eh/1-2113/92-28	
Subj:	A Few Observations, Suggestions, and about Triquint Fixes	**Date:**	August 26, 1992

Ref to two previous memos by the writer plus fax from DFP of Triquint

My Suggested Reason

As noted in one of my previous memos, I suspect that a lowered E mode device threshhold possibly operating in conjunction with sidegating due to manufacturing tolerances not being adequate and also in conjunction with hysteresis may be the culprit.

Triquint's Hypothesis (They know their product better than I do.)

Triquint thinks the problem relates to charge storage in the crystalline defects. Their solution is have a small amount of current flowing through the top of the off differential pair in the top of the cascode network which makes up the MUX which selects the clock or clock/2 signal. I have crudely drawn in the figure below what I believe they are telling me. The upper right side of the differential pair is the 'off' pair in this example and would represent, for example, clock/2. Without their fix, the current through either member of this differential pair cannot exist because the lower part of the cascode is open circuited (has not been selected by the select line which is in effect DSTOPBIT.

Triquint's Modification to the MUX Macro

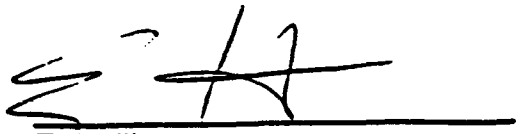
They intend to modify the MUX by adding a separate path -Vee to allow a small amount of current to flow even when that side is in the 'off' state.

My Concerns

Their theory is that this small amount of current flowing through the differential pair which is in the off state will overcome the problems arising from the crystalline defects.

I have two concerns about this modification. (But again, they know their product better than I do.) First I don't like the idea of feeding current through one or both sides of differential pair which is set up to be regenerative. Secondly, I especially don't like this when I suspect a degraded noise margin due to a suspected lowered threshhold of the E mode device and/or sidegating and hysteresis. My overriding concern is that while this may cure the problem in the lab, it may become a disaster in real life operation. (By the

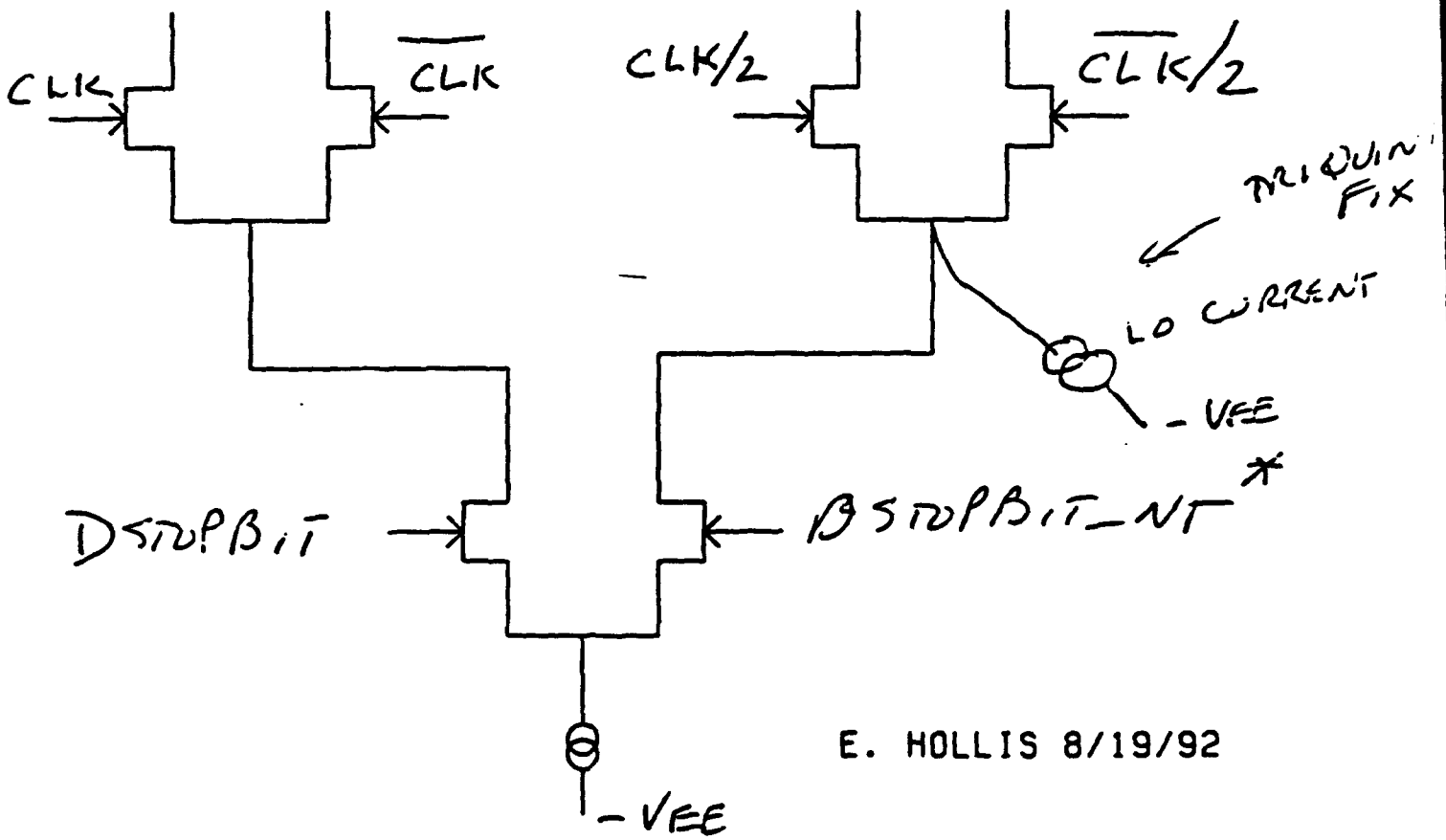
same token, we'll never get to real life operation if we don't allow the vendor to do what it thinks is best and if we keep raising too many problems whose probabilities of occurrence are not known.)



E. Hollis
Project Manager Custom VLSI
Microwave Technology Center

Distribution:

E. Bachelor
F. DeCaro
J. Sylvain
E. Wassung



E. HOLLIS 8/19/92

DRAIN RESISTORS AND SOURCE FOLLOWERS, ETC ARE NOT SHOWN AND ARE NOT NECESSARY FOR THIS EXAMPLE

* POLARITIES MAY BE REVERSED

APPENDIX B,
ATTACHMENT 3
LOCKHEED SANDERS BRIEFING NOTES
NASHUA MEETING
28 AUGUST 1992

Lockheed Sanders

AN/ALQ-126B(+)

PROGRAM DEVELOPMENT STATUS

28 AUGUST 1992

DEVELOPMENT PLAN

- **TWO PHASE PROGRAM**

  PHASE I ANALOG CONFIGURATION

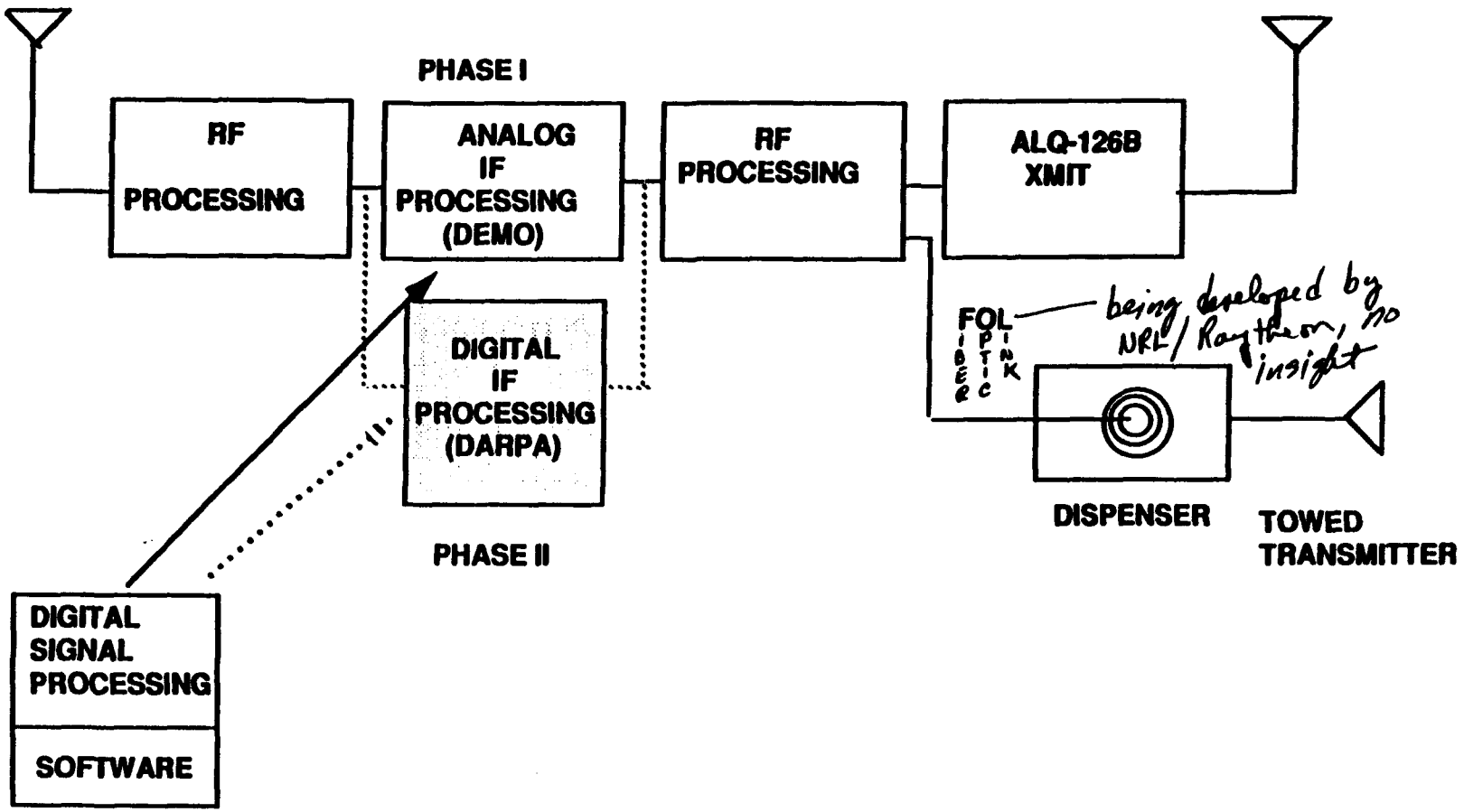
  - **PERMITTED SOFTWARE/HARDWARE DEVELOPMENTS WITH APPLICABILITY TO PHASE II**
  - **FLIGHT TESTABLE UNIT READY AT EARLY DATE (SUMMER'91)**

  PHASE II DIGITAL GaAs CONFIGURATION

  - **RETROFIT PHASE I CONFIGURATION WITH DIGITAL GaAs MODULE**
  - **ADDITIONAL SOFTWARE/HARDWARE INTERFACE EFFORTS**
  - **BASIS FOR PROPOSED SYSTEM SOFTWARE WITHIN EXISTING VOLUME**
  - December 1992 Bench Test

Lockheed Sanders

TWO PHASE PROGRAM ALLOWS EARLY TESTING



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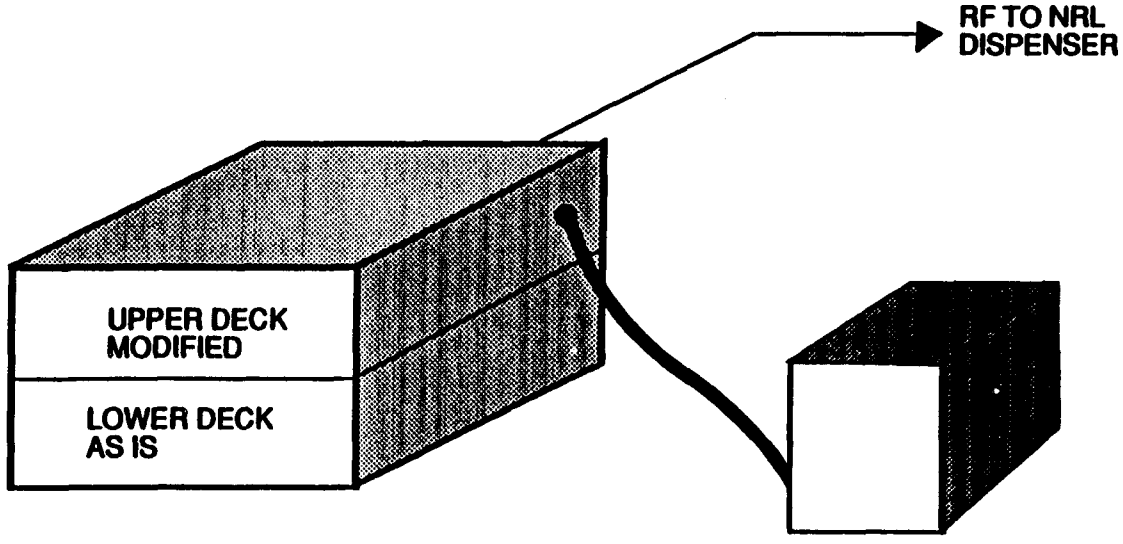
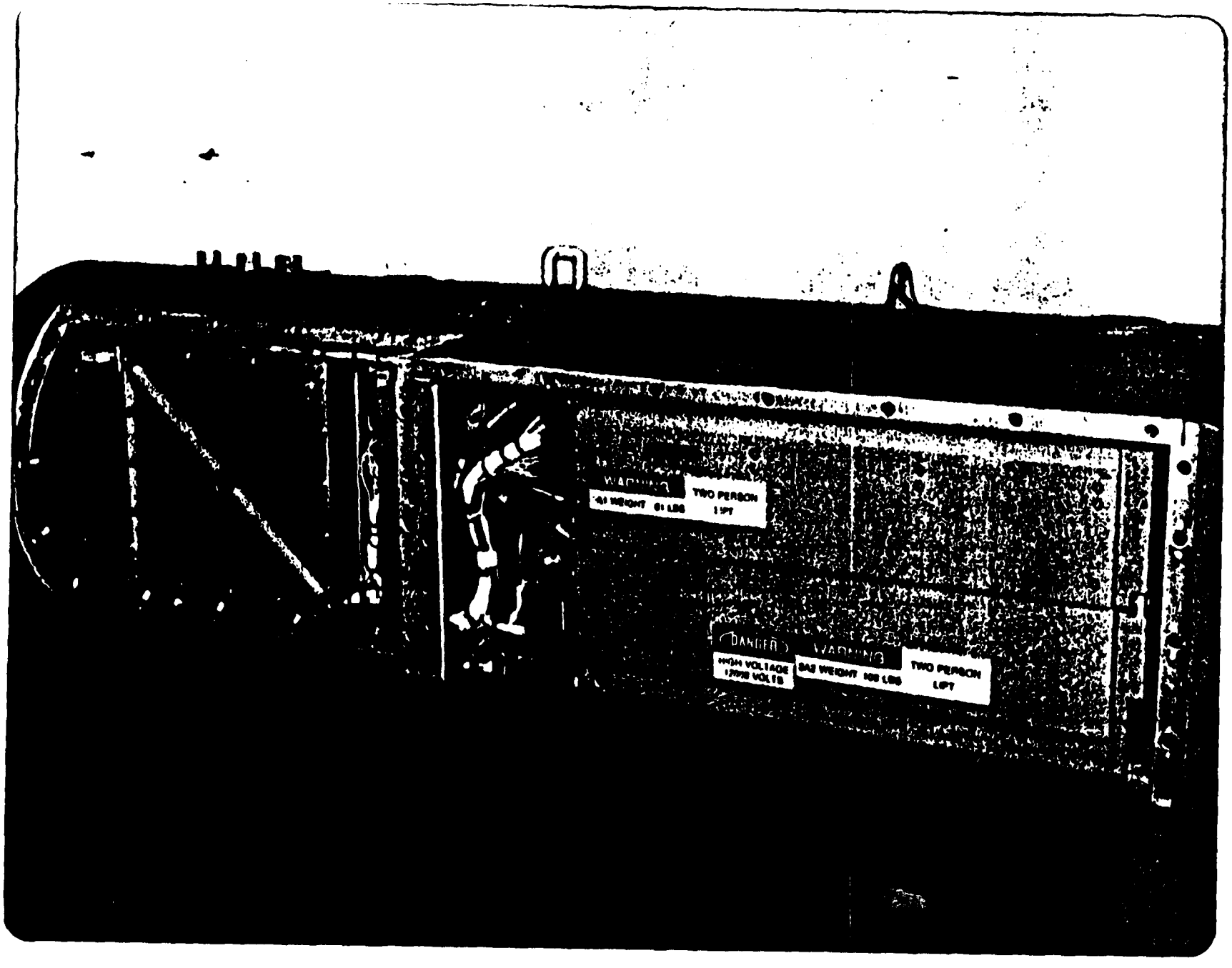
ALQ-126B(+) BRASSBOARD CONFIGURATION



O INSTALLATION
- IN ALQ-164 POD

IF PROCESSOR
PHASE I ANALOG
PHASE II DIGITAL GaAs


TWO PERSON
LIFT
DANGER
HIGH VOLTAGE
TWO PERSON
LIFT

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SYSTEM DESIGN APPROACH

- SYSTEM DESIGN HAS BEEN ANALYZED FOR BOTH PACKAGING AND THERMAL FEASIBILITY

- SYSTEM UPPER DECK DIMENSIONING HAS BEEN BASIS FOR DEVELOPMENT OF DGAS MODULE(S) FORM FACTOR

THERMAL ANALYSIS RESULTS

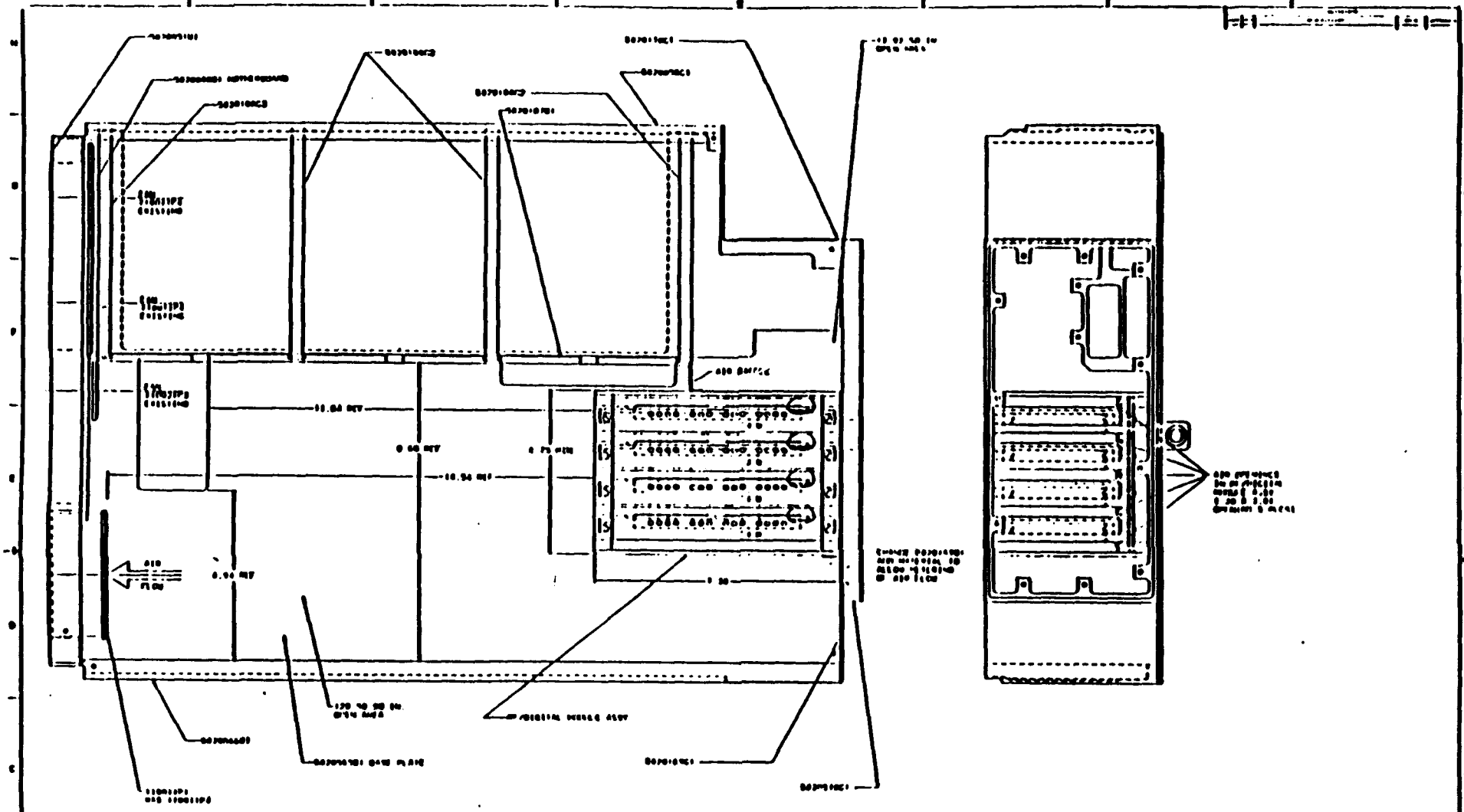
- ASSEMBLIES DESIGNED TO BE COOLED DIRECTLY AND INDIRECTLY
- MAXIMUM COMPONENT TEMPERATURES: (AT 70K FEET)

INDIRECT (CONDUCTION): 119 °C CASE TEMPERATURE

138 °C CHANNEL TEMPERATURE

DIRECT (FORCED CONVECTION): 108 °C CASE TEMPERATURE

125 °C CHANNEL TEMPERATURE



Lockheed Sanders

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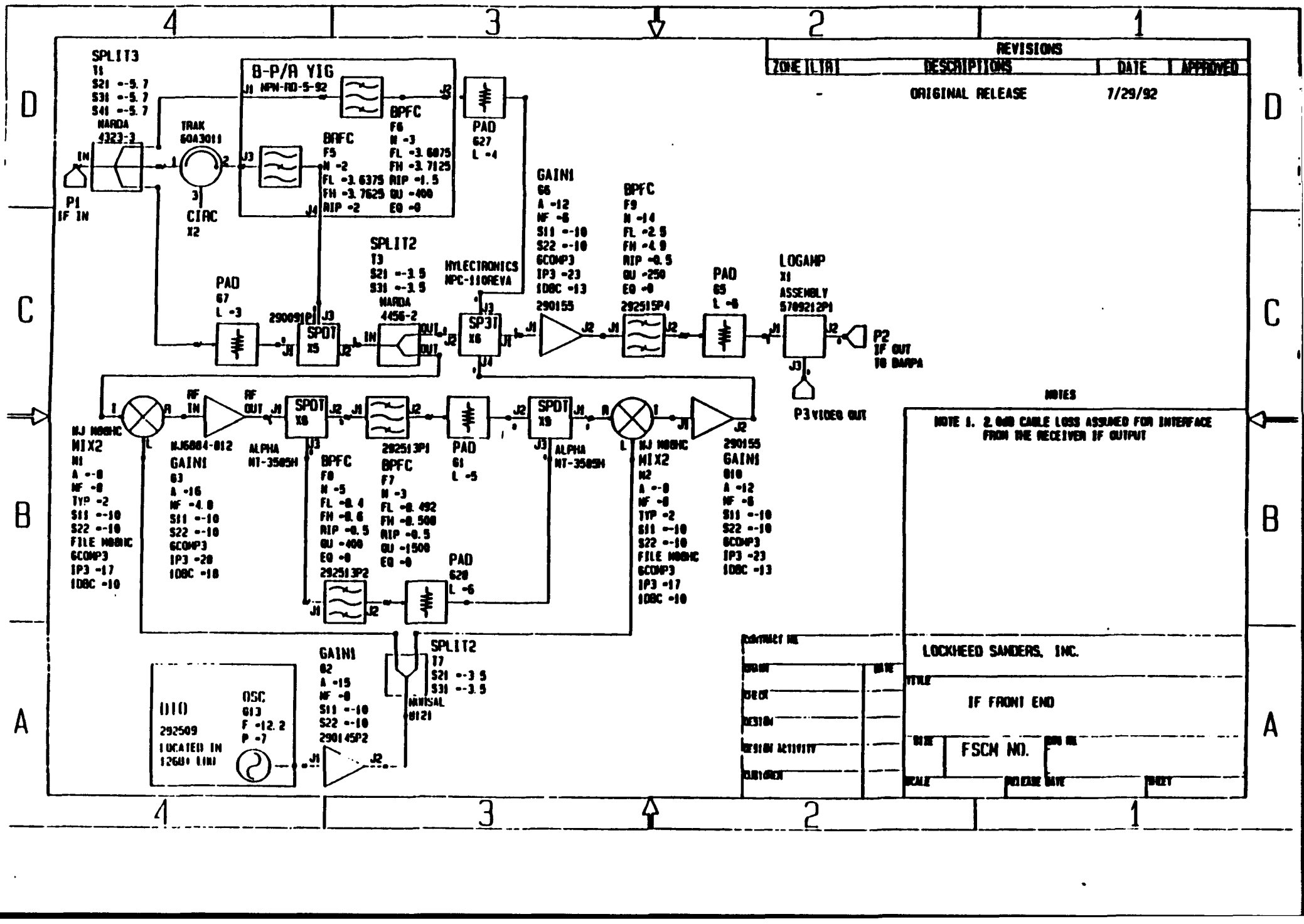
AN/ALQ-126B IRAD

FY'92 PROGRESS/ACCOMPLISHMENTS

- MICROWAVE INTERFACE TO GaAs IF PROCESSOR DEFINED
- DESIGN ANALYSIS OF THE IF FRONT END COMPLETED USING EESof's OMNISYS PROGRAM
  - SIGNAL TO NOISE RATIO
  - GAIN/POWER VERSUS FREQUENCY
  - SPURIOUS
  - TOI
- MICROWAVE COMPONENTS SPECIFIED
- MECHANICAL ASSEMBLY OF THE IF FRONT END STARTED
- INTERNAL SYSTEM REVIEW CONDUCTED 8/7


REVISIONS
ZONE | LTR | DESCRIPTIONS | DATE | APPROVED
- ORIGINAL RELEASE 7/29/92
SPLIT3
T1
S21 =-5.7
S31 =-5.7
S41 =-5.7
NARDA
4323-3
TRAK
60A3011
P1
IF IN
CIRC
X2
B-P/A YIG
J1 NPN-80-5-92
BPFC
F5
N =2
FL =3.6375
FH =3.7625
RIP =2
BPFC
F6
N =3
FL =3.6875
FH =3.7125
RIP =1.5
QU =400
EQ =0
PAD
627
L =4
PAD
67
L =3
SPOT
X5
SPLIT2
T3
S21 =-3.5
S31 =-3.5
NARDA
4456-2
MYLECTRONICS
MPC-110REVA
SP3T
X6
GAIN1
G6
A =12
NF =6
S11 =-10
S22 =-10
GCOMP3
IP3 =23
IDBC =13
290155
BPFC
F9
N =14
FL =2.5
FH =4.9
RIP =0.5
QU =250
EQ =0
PAD
65
L =6
LOGAMP
X1
ASSEMBLY
5709212P1
P2
IF OUT
TO DAMPA
P3 VIDEO OUT
NJ MODHC
MIX2
M1
A =-8
NF =8
TYP =2
S11 =-10
S22 =-10
FILE MODHC
GCOMP3
IP3 =17
IDBC =10
RF IN
RF OUT
NJ6884-012
ALPHA
MT-3505H
GAIN1
G3
A =16
NF =4.8
S11 =-10
S22 =-10
GCOMP3
IP3 =20
IDBC =18
SPOT
X8
BPFC
F8
N =5
FL =8.4
FH =8.6
RIP =0.5
QU =400
EQ =0
292513P2
292513P1
BPFC
F7
N =3
FL =8.492
FH =8.508
RIP =0.5
QU =1500
EQ =0
PAD
61
L =5
PAD
628
L =6
SPOT
X9
ALPHA
MT-3505H
NJ MODHC
MIX2
M2
A =-8
NF =8
TYP =2
S11 =-10
S22 =-10
FILE MODHC
GCOMP3
IP3 =17
IDBC =10
290155
GAIN1
G10
A =12
NF =6
S11 =-10
S22 =-10
GCOMP3
IP3 =23
IDBC =13
OIO
292509
LOCATED IN
12GHz LNA
OSC
G13
F =12.2
P =7
GAIN1
G2
A =15
NF =8
S11 =-10
S22 =-10
290145P2
SPLIT2
T7
S21 =-3.5
S31 =-3.5
MINISAL
8121
NOTES
NOTE 1. 2.0dB CABLE LOSS ASSUMED FOR INTERFACE FROM THE RECEIVER IF OUTPUT
LOCKHEED SANDERS, INC.
TITLE
IF FRONT END
FSCM NO.

Lockheed Sanders

DIGITAL GaAs IF PROCESSOR MODULE DEVELOPMENT STATUS

UP/DN CONVERTER

- IF FREQUENCY SCALING
- COMPLETELY ASSEMBLED/TESTED

LO/CLK

- PROVIDES LOCAL OSCILLATORS/SUBSYSTEM CLOCKS
- COMPLETELY ASSEMBLED/TESTED

BAND SELECT

- SELECTION OF ONE OF THREE IF SUBBANDS FOR DETECTED SIGNAL
- COMPLETELY ASSEMBLED/TESTED

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MODULE DEVELOPMENT STATUS (CON'T)

DIFM

- PROVIDES DIGITIZED FREQUENCY/PHASE DATA
- COMPLETELY ASSEMBLED/TESTED
  - ONLY 1 FUNCTIONALLY ACCEPTABLE DIFM-1 ASIC OUT OF 10 LOT

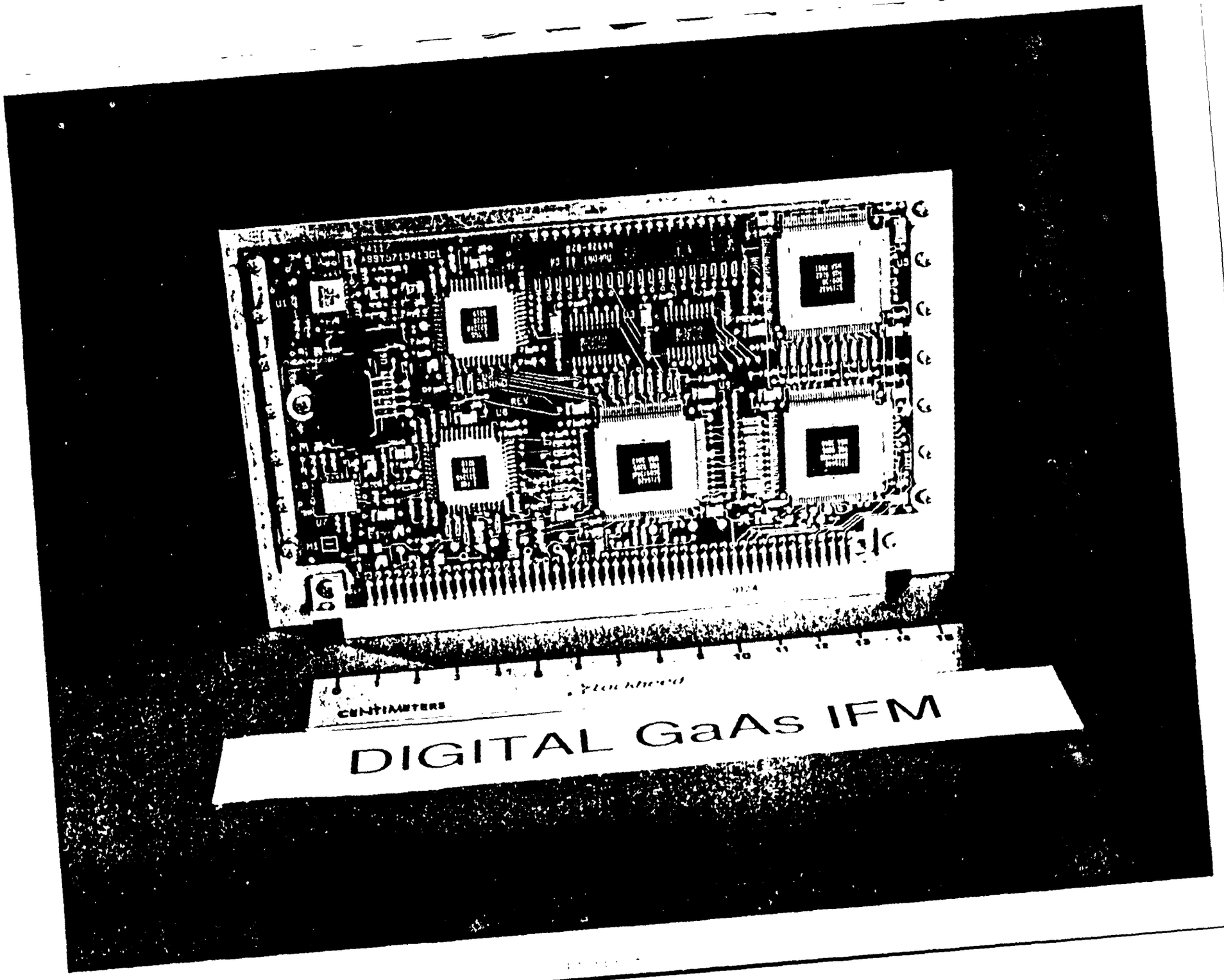
DSC

- SIGNAL RECONSTRUCTION FROM FREQUENCY/PHASE DATA
- PRINTED CIRCUIT BOARD FABRICATED
- MODULE BUILT-TO-SHORT . AWAITING DSC-3 ASIC(S) SCHEDULED FOR DELIVERY BY 9/4

DSC-3 = Combined function of DSC-1 & DSC-2

MEMORY - CMOS (TTL)

- PHASE DATA STORAGE/RECALL
- MODULE ASSEMBLED AND CURRENTLY IN TEST


CENTIMETERS
DIGITAL GaAs IFM

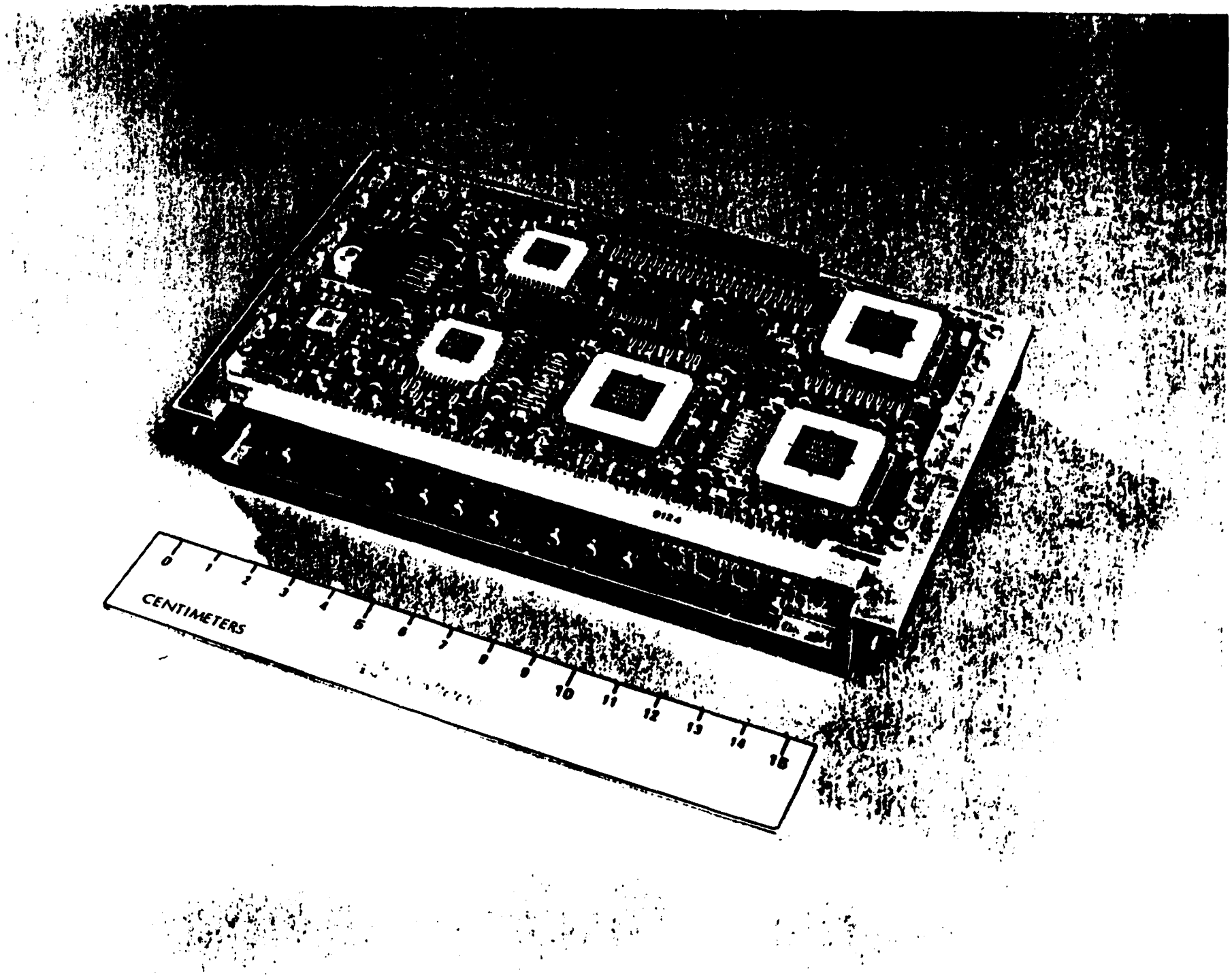


FIGURE 3

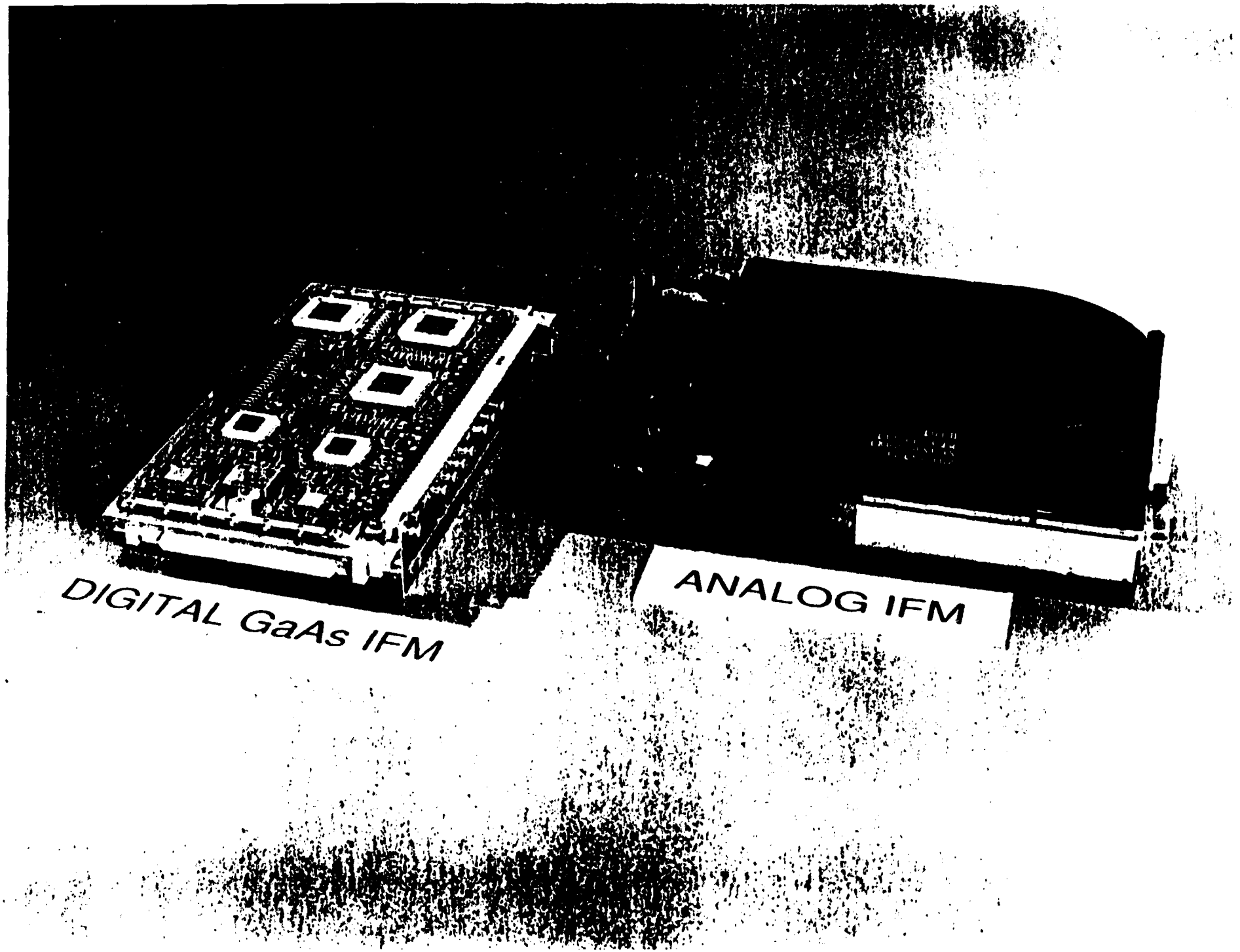


FIGURE 4

ASIC PROBLEM LOG

*DIFM-1	RESPONSIBILITY
• MACRO DEFICIENCY – Main problem	TRIQUINT
• A/D CLOCK POLARITY REVERSAL	TRIQUINT
• PHSDAT 0 (LSB) BANDWIDTH	TRIQUINT
• PL_MN POLARITY REVERSAL	SANDERS
• SDLSYNC NEEDS POLARITY REVERSAL	SANDERS

• SC-1	
• CRSFREQ6, CRSFREQ7, → FREQWD7, FREQWD8 TTL BUFFERS	SANDERS
• SCBDRV ERROR WINDOW WRONG REDUCE BY 1 CLOCK CYCLE	SANDERS
• SDLSYNC DUTY CYCLE VARIATIONS	TRIQUINT

DIFM-2

- (NONE TO DATE)

* WORK AROUNDS HAVE BEEN IDENTIFIED FOR NO IMPACT TO DEMONSTRATION

Lockheed Sanders

DARPA DIGITAL GaAs

REMAINING DELIVERABLES

- TWO QUARTERLY REPORTS THROUGH PROGRAM COMPLETION
  - ONE IN PROCESS OF PREPARATION
- FINAL ASIC/MODULE DESIGN SPECIFICATIONS
  - AT PROJECT COMPLETION
- TEST PLAN - IN TYPING
  - DUE 60 DAYS PRIOR TO TEST PLAN REVIEW (NOVEMBER)
  - BENCH DEMONSTRATION (DECEMBER)
- PROJECT FINAL REPORT
  - ROM COST DATA
  - RESULTS OF DEMONSTRATION TEST

Lockheed Sanders

DEMONSTRATION TASKS TO COMPLETE

- REVIEW DEMONSTRATION PROCEDURE WITH PROGRAM SPONSOR
- COMPLETE DSC MODULE ASSEMBLY/TEST
- MODULE LEVEL INTEGRATION
- IF PROCESSOR INTEGRATION
- IR&D SOFTWARE/HARDWARE IF PROCESSOR INTERFACE EFFORTS TO FACILITATE SYSTEM LEVEL DEMONSTRATION

Lockheed Sanders

SYSTEM REQ. REVIEW

GOALS FOR BENCH DEMONSTRATION:

- DARPA BENCH DEMONSTRATION IS "NOT" A CONDITION FOR ACCEPT/REJECT
- CONTRACTUAL REQUIREMENT TO DEMONSTRATE IF-PROCESSOR ONLY
- INTENT TO PERFORM SYSTEM LEVEL DEMONSTRATION. GAIN DARPA ASSISTANCE IN PROMOTION OF SYSTEM UPGRADE WITHIN NAVY COMMUNITY
- CONDUCT ALL EFFORTS IN ANTICIPATION OF FLIGHTS TEST
  - HARDWARE DESIGN
  - SOFTWARE DEVELOPMENT

Lockheed Sanders

SYSTEM REQ. REVIEW

PROPOSED BENCH DEMONSTRATION: (W/COMPARISON TO PRODUCTION ALQ-126B)

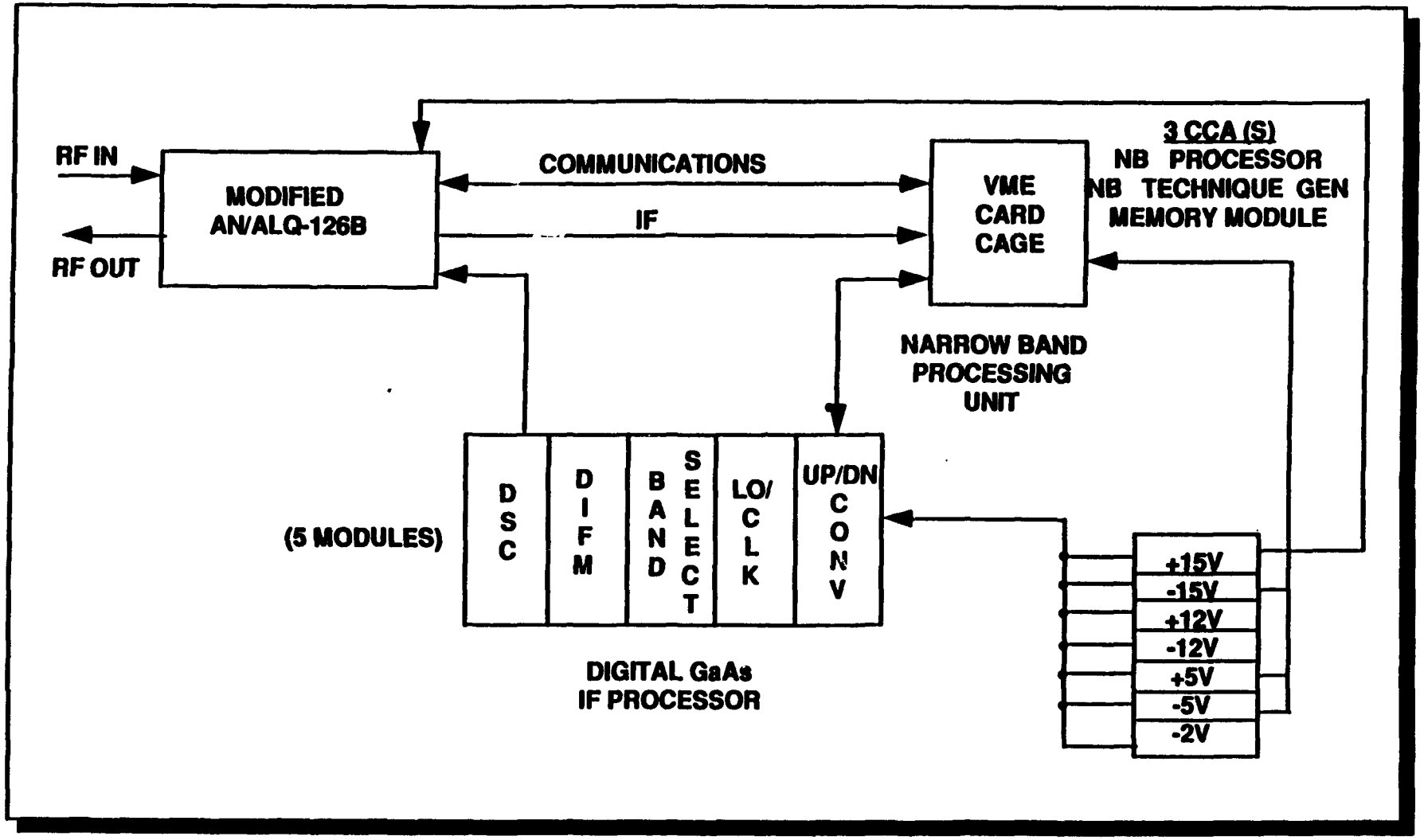
SYSTEM RESPONSE TO THE FOLLOWING:

1. SINGLE HB PULSED THREAT → PRESENT SYSTEM CAPABILITY
2. TWO PULSED THREATS → DSC MULTIPLEXING FOR TWO TRANSPONDER ASSIGNMENTS
3. SINGLE COHERENT PULSE DOPPLER → FIXED RANGE/FIXED VELOCITY TECHNIQUE
   COMPARE INPUT/OUTPUT FREQ. SPECTRUM
4. PULSE DOPPLER WITH CW → CW LOCATED OUTSIDE PRODUCTION SYSTEM REJECT FILTER
5. MULTIPLE ENVIRONMENT

   1 - PULSE DOPPLER, 1 - CW, 2 PULSED (TRANSPONDER)

Lockheed Sanders

BENCH DEMONSTRATION



Lockheed Sanders

SYSTEM REQ. REVIEW

REQUIREMENTS FOR FLIGHT TEST:

SYSTEM INSTALLATION

- **NEEDS TO BE IDENTIFIED**
- **ASSUMED ALLOCATION (2.3 CU. FT. 126B + 1 CU. FT. EXT. BOX)**
- **ACCOMMODATE INTERNAL AIRFRAME OR ALQ-164 INSTALL**

INTEGRATION TO OFFBOARD UNIT

- **CURRENTLY ANTICIPATING FUNDING FOR DETAILED STUDY OF INTERFACE TO NRL OFFBOARD**
- **ACTUAL EFFORT SHOULD BE INITIATED WITHIN FIRST QUARTER '93**

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TASKS TO PREPARE FOR FLIGHT

- PACKAGE BENCH DEMO CONFIGURATION FOR FLIGHT
- DEFINE FLIGHT TEST
- IDENTIFY PLATFORM/INSTALLATION (I.e. INTERNAL/POD)
- LIMITED ENVIRONMENTAL TEST TO ENSURE FLIGHT WORTHINESS
- TRANSMITTER INTERFACE DEVELOPMENT/BENCH INTEGRATION

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AN/ALQ-126B(+)

SYSTEM UPGRADE

28 AUGUST 1992

DARPA DIGITAL GaAs PROGRAM
AN/ALQ-126B

- TECHNOLOGY DEVELOPMENT PROGRAM SPONSORED BY NAVAIR TO DEMONSTRATE AND PROTOTYPE ELECTRONIC FUNCTIONS IN DIGITAL GaAs TECHNOLOGY TO SIGNIFICANTLY ENHANCE CAPABILITY OF THE PRESENTLY FIELDED SYSTEM

  - DEVELOP A COST-EFFECTIVE APPROACH TO PROVIDE ECM CAPABILITY AGAINST NEW CLASS EMITTERS
  - ACCOMMODATE MODIFICATIONS WITHIN VOLUME OF CURRENT SYSTEM FACILITATED BY DIGITAL GaAs MODULES

PROGRAM GOALS FOR ALQ-126B DGAS

- PROVIDE AFFORDABLE ECM UPDATE FOR AIRCRAFT WHICH WILL CARRY THE ALQ-126B
- IMPLEMENT IMPROVED CAPABILITY AGAINST
  - CW/PD THREATS
  - MONOPULSE
  - MULTIPLE SIGNAL ENVIRONMENT
- MINIMIZE AIRCRAFT GROUP A CHANGES

ENHANCED ALQ-126B CONCEPT

ENHANCED ALQ-126B CONCEPT

- MODIFY UPPER DECK WITH DIGITAL GaAs MODULES
  - INCORPORATES PD/CW PROCESSING CAPABILITY
  - IMPROVED MULTIPLE SIGNAL HANDLING
- NO CHANGE TO LOWER (TRANSMITTER) DECK
- MINIMAL CHANGE TO GROUP A RF XMISSION LINES
- INTERFACE ALQ-126B WITH IDAP PROGRAM VIA RF LINK TO OFF-BOARD SYSTEM
- TRANSMIT ON-BOARD/OFF-BOARD VS. PULSE THREATS
- TRANSMIT "SMART" OFF-BOARD VS. CW/PD THREATS

ALQ-126B ENHANCED CAPABILITIES

TACTICAL AIRCRAFT JAMMER REQUIREMENTS FOR 1990's

- NEWER THREATS HAVE MONOPULSE CAPABILITY
- OLDER THREATS REMAIN IN INVENTORY THRU 2000
- TACTICAL AIRCRAFT NEED ECM UPGRADES TO COUNTER MONOPULSE
- MANY MONOPULSE ECM TECHNIQUES ARE AVAILABLE
  OFF BOARD DECOY IS MOST AFFORDABLE AT LOWEST RISK

- OFF-BOARD DECOYS WON'T COUNTER OLDER THREATS AND FACE INTEGRATION PROBLEMS WITH ON-BOARD CW/PD JAMMERS

- THEREFORE-

A COMBINATION OF ON-BOARD PULSE JAMMING FOR OLDER THREATS AND OFF-BOARD JAMMING FOR NEWER THREATS IS AN EXCELLENT SOLUTION

HD

POTENTIAL PLATFORMS WITH ALQ-126B & TOWED TRANSMITTER

		NO OF A/C	STATUS
USN			
	F-18A/B	400	•ALL AIRCRAFT HAVE ALQ-126B
	*A-6E(2 PER AC)	200 (400)	
	F-14A/A+	200	
USMC	AV-8B W/ALQ-164	70	
INTERNATIONAL	F-18 CAN, AUS, SPAIN	200	
	TOTAL	1270	CANDIDATES FOR ALQ-126B DGAS/TT

* (2) ALQ-126B (s) PER AIRCRAFT - UTILIZE EXISTING LOWER DECKS
  ALE-50 INSTALL ALREADY PLANNED FOR PLATFORM

HD

TASKS TO ENHANCE ALQ-126B

- DARPA CONTRACT
  - DEVELOP CHIPS AND MODULES COMPATIBLE WITH ALQ-126B
    4 CHIPS 5 MODULES TOTAL - 2 GaAs MODULES
    BENCH DEMONSTRATION 4TH QUARTER '92

- LOCKHEED SANDERS ALQ-126B IR&D
  - TWO PHASED APPROACH FOR EARLIER IMPLEMENTATION
  - DEMONSTRATE SYSTEM LEVEL CAPABILITY
    PHASE I - ANALOG DIFM & DRFM SUCCESSFULLY BENCH TESTED SUMMER '91
    - AVAILABLE FOR FLIGHT TEST UNTIL GaAs RETROFIT WAS INITIATED (JULY '92)

    PHASE II - RETROFIT SYSTEM WITH DARPA GaAs DEVELOPMENTS
    - READY FOR FLIGHT 2ND QUARTER '93 (Calendar 1993)
    - REQUIRES INTEGRATION TO PD/CW TRANSMITTER

- NRL TOWED TRANSMITTER DEVELOPMENT
  - DEVELOPS DECOY AND COMMUNICATIONS LINKS
  - INTERFACE WITH ALQ-126B
  - FLIGHT TEST TO DEMONSTRATE COMMUNICATIONS LINK

ALQ-126B CAPABILITIES ENHANCEMENT

- COMMITMENT TO ENHANCEMENT OF THE ALQ-126B

- DARPA CONTRACT FOR GaAs INSERTION	$3.2M
- CONTRACTOR IRAD FOR SYSTEMS MODS	2.0
	$5.2M

- INTENT IS TO FIELD DARPA TECHNOLOGY DEVELOPMENTS
  - UPGRADES ARE SOLD THROUGH DEMONSTRATION
  - ALQ-126B DGAS NEEDS NAVAIR FLIGHT TEST INTEREST

HD

ENHANCED ALQ-126B

SUMMARY

- EXISTING ON-BOARD ECM SYSTEMS REQUIRE ENHANCEMENT
  - ENHANCED ALQ-126B IS COST EFFECTIVE SOLUTION
- ENHANCED ALQ-126B + OFF-BOARD + RF LINK PROVIDE A ROBUST SUITE
  - PREFERRED MONOPULSE SOLUTION
  - RAIL KEEPING TECHNIQUES
  - ROBUST MISSILE END GAME JAMMING
- ENHANCED ALQ-126B REQUIRES MINIMAL A KIT MODIFICATIONS
- OFF-BOARD PROGRAM PROCEEDING INDEPENDENT OF ALQ-126B(+)

RECOMMENDATION

SUPPORT THE AN/ALQ-126B DGAS EFFORT

- **NRL COORDINATION FOR SYSTEM/DECOY INTERFACE**
- **BENCH TEST RF/FIBER OPTIC LINK**
- **IDENTIFY TIME FRAME/PLATFORM/RESOURCES FOR FLIGHT TEST**

PROVIDES COST EFFECTIVE ECM UPDATE TO PROVEN FIELDED SYSTEM

SCHEDULE

Calendar Years

	1991				1992				1993			
	First	Second	Third	Fourth	First	Second	Third	Fourth	First	Second	Third	Fourth
PHASE I (ANALOG SYSTEM)												
BENCH DEMO		▼										
AVAILABLE FOR FLIGHT			———	———	———	———	▼					
PHASE II (DGAS SYSTEM)												
GaAs RETROFIT						▲	———	▽				
BENCH DEMO								▽				
TRANSMITTER INTEGR. FLIGHT READY				-						△		

HD

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DEVELOPMENTS WITH NRL

- SUCCESSFUL BENCH TESTING CONDUCTED 4TH QUARTER '90 AT AFEWES WITH AN/ALQ-126B
- PLANNED FOLLOW-ON FLIGHT TESTING CANCELLED DUE TO IDENTIFICATION OF POTENTIAL ALTERNATE SYSTEM FOR TEST
- RECENTLY REQUESTED FOR ROM TO CONDUCT STUDY OF DETAILS OF SYSTEM/FOL/TT INTERFACE
  - CONTRACT IN DEFINITIZATION PROCESS
- UPON COMPLETION OF STUDY NEED TO EXPEDITE ACTUAL BENCH INTEGRATION IN PREPARATION FOR FLIGHT

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MARKETING STRATEGY

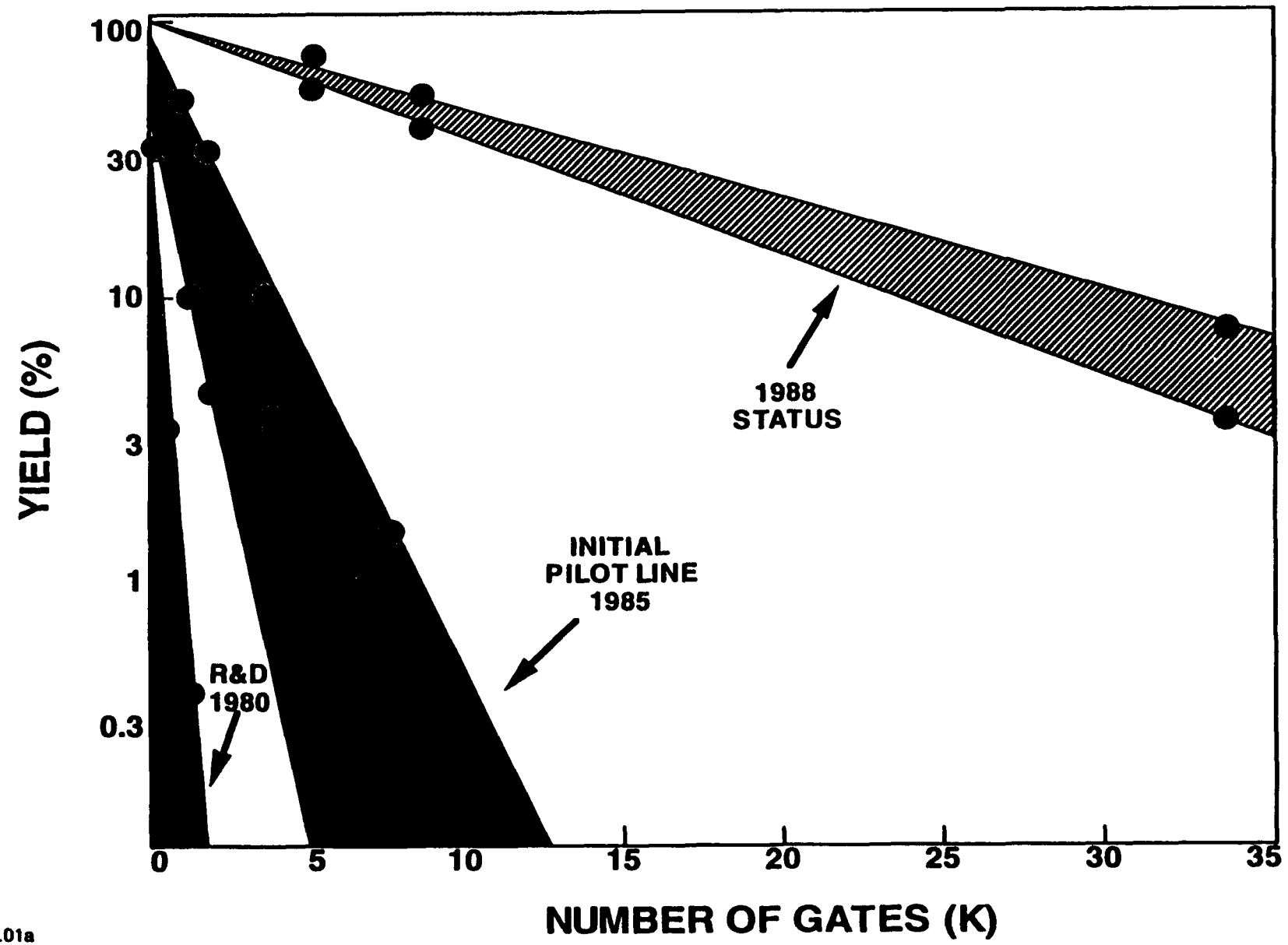
- AN/ALQ-126B(+) HAS BEEN PROPOSED AS COST-EFFECTIVE ECM UPDATE FOR NON-ASPJ AIRCRAFT
- NEED TO CULTIVATE NRL TOWED TRANSMITTER DEVELOPMENT/INTEGRATION
- IN PROCESS OF APPLYING FOR RELEASE OF BRIEFING MATERIAL TO PRESENT TO FOREIGN CUSTOMERS
- SANDERS CONTINUES TO INVEST IR&D FUNDS TO FACILITATE SYSTEM LEVEL DEMONSTRATION - BUT NEEDS CUSTOMER INTEREST/SUPPORT FOR FLIGHT TEST
- IR&D FUNDS ARE ALSO BEING INVESTED TO DEMONSTRATE AN/ALQ-126B IN AIR FORCE F-16. NATURAL FOLLOW-ON WOULD BE ALQ-126B(+)

APPENDIX C
BRIEFING ON
DIGITAL GaAs INSERTIONS:
A RETROSPECTIVE
20 NOVEMBER 1992

DIGITAL GaAs INSERTIONS: A RETROSPECTIVE

Zachary J. Lemnios

DIGITAL GaAs YIELD VS. COMPLEXITY



INSERTION DEMONSTRATION OF DIGITAL GaAs TECHNOLOGY

GOALS

- ADD OPERATIONAL CAPABILITY TO FIELDED PLATFORMS
  - — LESS COSTLY, MORE RAPID THAN DEVELOPING AND DEPLOYING NEW SYSTEMS
- KEEP U.S. MANUFACTURING LEAD IN DIGITAL GaAs
  - — REQUIRES MUCH MORE RAPID DEVELOPMENT OF MILITARY MARKETS THAN "BUSINESS AS USUAL"

INSERTION DEMONSTRATION OF DIGITAL GaAs TECHNOLOGY

APPROACH

- SELECT 6-10 TRAILBLAZER PROJECTS BASED ON:
  - TECHNICAL APPROACH
  - MILITARY PAYOFF OF INSERTION
  - LIKELIHOOD OF ACHIEVING INSERTION INTO SYSTEM
- ESTABLISH 3-WAY PARTNERSHIPS
  - CONTRACTOR
  - MILITARY SERVICE PROGRAM OFFICE
  - DARPA
- DARPA SUPPORTS INITIAL HIGH-RISK DEMONSTRATION
- SERVICE PROGRAM OFFICE
  - MONITORS DEMO EFFORT
  - FIELD TESTS AND QUALIFIES
  - PROCURES/INSTALLS UPGRADE

INSERTION DEMONSTRATIONS OF DIGITAL GaAs TECHNOLOGY

COMPANY	SUBSYSTEM	PLATFORM AND APPLICATION	GaAs PAYOFF
		INTELLIGENCE AND SURVEILLANCE	
E-SYSTEMS	DISTRIBUTED ARRAY PROCESSOR	AIR FORCE RC-135 RECONNAISSANCE AIRCRAFT	PROCESS SIX TIMES AS MANY SIMULTANEOUS SIGNALS AT 300 LBS LESS WEIGHT
MARTIN MARIETTA	ON BOARD PROCESSOR	SPACECRAFT	INCREASE FROM 75 MOPS TO 560 MOPS WITH NO CHANGE IN SOFTWARE
TEXAS INSTRUMENTS	SIGNAL PROCESSOR	NAVY P-3C AN/APS-137 SURFACE SEARCH RADAR	SIGNIFICANT IMPROVEMENT IN ISAR IMAGE RESOLUTION
GRUMMAN	RADAR PROCESSOR	NAVY E-2C AN/APS-145 AIRBORNE EARLY WARNING RADAR	45% GREATER RANGE; 35% SMALLER TARGETS
		WEAPONS AND COMBAT SUPPORT	
McDONNELL DOUGLAS	IMAGE PROCESSOR	ARMY OH-58D SCOUT HELICOPTER	TRACK-WHILE-SCAN; MOVING TARGET INDICATOR; MULTIPLE TARGET TRACKING
HONEYWELL	DIGITAL MAP COMPUTER	NAVY/MARINE CORPS TACTICAL A/C NAVIGATION	REAL-TIME MISSION REPLANNING; LOW-ALTITUDE TERRAIN AVOIDANCE
MARTIN MARIETTA	SIGNAL PROCESSOR	ARMY LONGBOW RF HELLFIRE MISSILE SEEKER	LOWER UNIT COST AT REDUCED WEIGHT AND VOLUME; IMPROVED LETHALITY
		ELECTRONIC WARFARE	
KOR ELECTRONICS	DIGITAL RF MEMORY	NAVY ULQ-21 TARGET DRONE ECM	LOWER UNIT COST AND IMPROVED TRAINING REALISM
ITT AVIONICS	DIGITAL RF MEMORY	ARMY AN/ALQ-136 AIRCRAFT ECM	COUNTER NEW THREATS WITHIN WEIGHT AND POWER CONSTRAINTS
SANDERS ASSOCIATES	SIGNAL PROCESSOR	NAVY AN/ALQ-126B TACTICAL AIRCRAFT ECM	COUNTER NEW THREATS WITHIN WEIGHT AND POWER CONSTRAINTS
		COMMUNICATIONS	
E-SYSTEMS	MODEM AND FREQUENCY SYNTHESIZER	ARMY AN/PRC-126 COMMUNICATIONS	ANTI-JAM FREQUENCY HOPPING; COMPATIBILITY WITH SINCGARS

XX1096(11)8-11-89

DIGITAL GaAs INSERTIONS: DARPA IMPACT

DIRECT MILITARY PAYOFFS

- Navy (PMA-240) negotiating production contract with TI for digital GaAs processor for all P-3Cs; US Coast Guard will also upgrade their ISAR with the same GaAs processor
- ATCOM Kiowa Warrior Program Office negotiating production contract with McDonnell Douglas for digital GaAs processor for mast mounted sight
- CECOM will use ITT's GaAs DRFM in Advanced Threat Radar Jammer (ATRJ) (ITT has developed an integrated analog and digital RF GaAs chip to be used in an ATRJ upgrade)
- Next-generation Navy satellites will use GaAs processors
- Navy (PMTC, Point Mugu) will use KOR DRFM in ECM training drones
- NAVAIR is considering AN/ALQ-126B as replacement if the Airborne Self Protection Jammer (ASPJ) is cancelled
- CECOM and E-Systems will produce an all-digital radio based on GaAs components

DIGITAL GaAs INSERTIONS: DARPA IMPACT

INDUSTRY INFRASTRUCTURE

- TriQuint offering the Lockheed Sanders-designed DAC as a standard product
- Vitesse and MDESC negotiating on MDESC-designed signal processor as a standard product
- ITT using digital GaAs technology in the F-22 program
- Two digital GaAs Design Centers have been established – Martin Marietta, Denver and KOR Electronics
- TI's digital GaAs technology is being used in prototypes at 4 DoD labs
- Martin Marietta, MDESC, TI, & E-Systems are each pursuing military satellite applications of digital GaAs
- All systems companies continue to design digital GaAs into their products

APPENDIX D
SCHEDULE OF REVIEWS AND DEMONSTRATIONS FOR THE TRANSITION OF OPTICAL PROCESSORS TO SYSTEMS (TOPS) PROGRAM OCTOBER 1992–DECEMBER 1994

TOPS Schedule of Reviews and Demos

Note: Harris has stopped work on the EWC/PDF contract. Harris and NRL are meeting this week to work out a solution. Future review and demo dates for EWC/PDF are therefore TBD.

October 1992

Harris (Melbourne)	OAM	Dan Beard 407-727-6176	"informal" review w/ Rome 26,27 October
Hughes (Fullerton)	Phased Arrays	J. J. Lee 714-732-6828	"informal" review w/ N. Bernstein, 28 Oct

November 1992

TI (Dallas)	Phased Arrays	Chris Hemmi 214-575-6269	semi-annual review (early Nov.)
GE (Syracuse)	Null Steering	Dan Friedman 315-456-4952	quarterly review
TBE (Huntsville)	Pattern Recogn.	Charles Hester 205-726-1999	review
BDM (McLean)	SAR	Mike Haney 703-848-5854	demo

December 1992

Nothing scheduled.

January 1993

Martin Mar. (Denver)	Pattern Recogn.	Scott Lindell 303-971-3253	PDR
Dynetics (Huntsville)	Pulse Compress.	Neil Mohon 205-922-9230	PDR; demo 1-D correlator (25-29 Jan 93)
Hughes (Fullerton)	Phased Arrays	J. J. Lee 714-732-6828	"informal" review w/ N. Bernstein

TOPS Schedule of Reviews and Demos

February 1993

OPTICS REVIEW 8-12 Feb 93 Hilton Inn, Hilton Head Island, SC

ERIM/ BDM	SAR	Ivan Cindrich Mike Haney	system review (1st week of Feb.)
TBE (Huntsville)	Pattern Recog.	Charles Hester 205-726-1999	final build

March 1993

GE (Syracuse)	Null Steering	Dan Friedman 315-456-4952	quarterly review (Mar/Apr 93)
Hughes (Fullerton)	Phased Arrays	J. J. Lee 714-732-6828	CDR, lab demo possible (Mar/Apr 93)

April 1993

SPIE/TOPS 12 April 93 Marriott World Center, Orlando, FL

May 1993

TI (Dallas)	Phased Arrays	Chris Hemmi 214-575-6269	semi-annual review (early May)

June 1993

Martin Mar. (Denver)	Pattern Recog.	Scott Lindell 303-971-3253	Flyable Prototype Environ. Eval. (at MM)

July 1993

GE (Syracuse)	Null Steering	Dan Friedman 315-456-4952	quarterly review perhaps lab demos

TOPS Schedule of Reviews and Demos

August 1993

Martin Mar. (Denver)	Pattern Recogn.	Scott Lindell 303-971-3253	CDR
Dynetics (Huntsville)	Pulse Compress.	Neil Mohon 205-922-9230	review; demo 2-D correlator
ERIM/ BDM	SAR	Ivan Cindrich Mike Haney	CDR (1st week of Aug.)

September 1993

Nothing scheduled.

October 1993

TI (Dallas)	Phased Arrays	Chris Hemmi 214-575-6269	semi-annual review, demo prototype chip (Oct/Nov 93)

November 1993

GE (Syracuse)	Null Steering	Dan Friedman 315-456-4952	quarterly review; possible processor demo
Martin Mar. (at MICOM)	Pattern Recogn.	Scott Lindell 303-971-3253	SPOTR delivery

December 1993

Nothing scheduled.

January 1994

Hughes (Fullerton)	Phased Arrays	J. J. Lee 714-732-6828	system demo (sometime early 94)
Martin Mar. (at MICOM)	Pattern Recogn.	Scott Lindell 303-971-3253	tower test

TOPS Schedule of Reviews and Demos

February 1994

Martin Mar. (at MICOM)	Pattern Recogn.	Scott Lindell 303-971-3253	flight test
Dynetics (Huntsville)	Pulse Compress.	Neil Mohon 205-922-9230	review, integrated system demo

March 1994

Nothing scheduled.

April 1994

Dynetics (at MICOM)	Pulse Compress.	Neil Mohon 205-922-9230	MICOM radar demo
ERIM/ BDM	SAR	Ivan Cindrich Mike Haney	system review (1st week of Apr.)

May 1994

Dynetics (at CECOM)	Pulse Compress.	Neil Mohon 205-922-9230	CECOM ESM demo

July 94

Dynetics (Huntsville)	Pulse Compress.	Neil Mohon 205-922-9230	final review

December 1994

ERIM/ BDM	SAR	Ivan Cindrich Mike Haney	system review/demo (1st week of Dec.)